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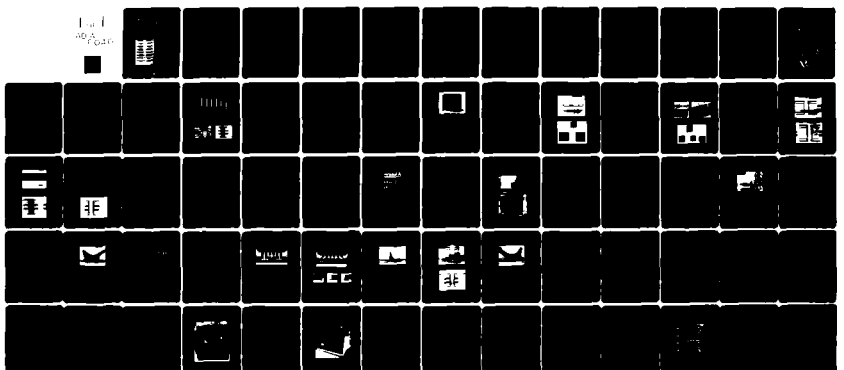

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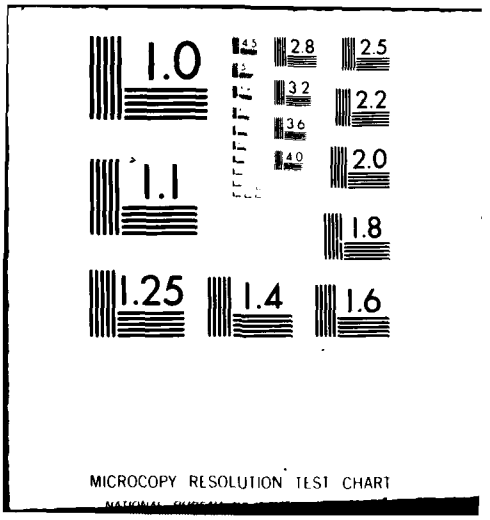
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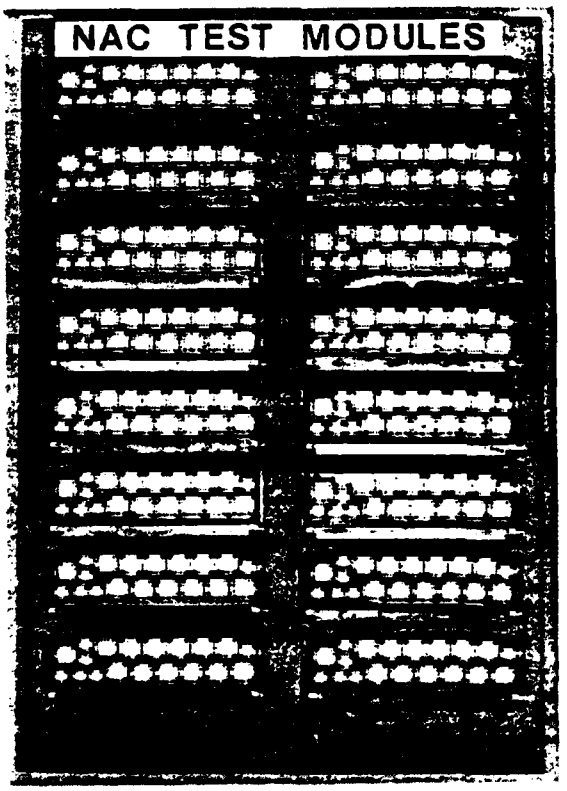
Metal Core Epoxy Glass Circuit Board Evaluation Program

FINAL REPORT



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DECEMBER 1981

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Leadless hermetic chip carriers are becoming the standard IC package. Their use in combination with epoxy glass PWB's results in unreliable solder joints because of the thermal expansion mismatch between the HCC and epoxy glass PWB. The problem is manifested when assemblies are subjected to repeated thermal excursions.

This report describes an approach to reducing the CTE of the epoxy glass PWB (15 to 20 ppm/°C) to a value close to the CTE of the ceramic HCC (6 to 7 ppm/°C). This is accomplished by laminating a low expansion metal layer internal to the multilayer board. This stabilized MLB reduces the stresses incurred in the solder joints, and subsequently reduces the number of fractures due to solder fatigue when thermally cycled.

Test methods, test results and failure analysis are also included in this report.

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1.0 CONCLUSION

Combining Alloy 42 with typical epoxy glass MLB's reduces the MLB composite CTE to a value close to that of the hermetic chip carrier CTE. Thermal expansion measurements demonstrated the epoxy glass MLB has a typical CTE of 18 ppm/^{o}C and a metal core epoxy glass MLB has a typical CTE of 8 to 9 ppm/^{o}C. This is close to the HCC ceramic which has a CTE of 6.8 ppm/^{o}C.

Utilization of the metal core epoxy glass MLB with HCC's is significantly more reliable than utilization of epoxy glass MLB's with HCC's. Thermal cycle testing of test samples demonstrated a 4:1 improvement of the metal core epoxy glass MLB's over similar epoxy glass MLB's when using first solder joint failure as an acceptance criteria. At the conclusion of 1000 temperature cycles between -55^{o} and $+125^{o}$C, 26% of the metal core epoxy glass MLB/HCC solder joints had failed while at the conclusion of 200 temperature cycles, 75% of the epoxy glass MLB/HCC solder joints had failed.

The metal core epoxy glass MLB permits designing an MLB with different CTE's. This accommodates a reliable HCC/MLB solder joint which requires an MLB with a low CTE, and also a reliable connector/MLB solder joint which requires an MLB with a high CTE. Tests at NWSC showed that a similar connector mounted to a ceramic substrate evidenced solder joint failures after less than twenty temperature cycles between -55^{o}C and $+125^{o}$C. Metal core MLB's utilized on the program withstood 300 temperature cycles before a failure. This is a 15:1 improvement.

The addition of the Alloy 42 layers to the epoxy glass MLB does not appear to impact the reliability of the plated-through holes. No failures were observed among the plated-through holes located within the Alloy 42 area. Nonfunctional pads are required in order to obtain this reliability. Unsupported plated-through holes in the connector area experienced a failure after 400 thermal cycles.

In conclusion, the metal core epoxy glass MLB is a reliable interconnection substrate compatible with leadless HCC's and the SEM Format B 100 pin connector.

2.0 INTRODUCTION

2.1 NEED FOR CHIP CARRIER INTERCONNECTION TECHNOLOGY

Hermetic chip carriers, HCC's, are being used by the electronics industry as a means of increasing component density and maintaining or reducing assembly costs. Studies indicate that the HCC package is rapidly becoming a standard and that by the mid 1980's, 80% to 90% of the electrical functions will be available in this configuration. Discussions with various IC vendors have substantiated this premise for the future of HCC application. Semiconductor manufacturers are actively pursuing studies to determine the need and anticipated use of devices for future application.

Anticipating the HCC would become the new IC standard package, Ordnance Systems' initiated activity on HCC interconnection substrate development. Initially, the activity centered on investigating alternate materials and fabrication techniques which would satisfy the following requirements:

a. Ensure economical production techniques comparable to present PWB cost

b. Accommodate a large area of applications

c. Accommodate through-hole and planar component mounting

d. Ensure materials are available and readily processable

e. Accommodate high density electronic packaging

f. Ensure reliable solder connections

g. Facilitate short-term prototype development cycles

Most of these criteria were met by ceramic thick-film technology, but this technique posed a problem at the SEM connector/ceramic interface and required up to 38 to 40 processing steps in order to ensure a component density comparable to a four-layer PWB. Thus, material cost and processing time become excessive in comparison to PWB technology.

Epoxy glass and polyimide glass PWB's meet most of these criteria except for the reliable solder joints between the HCC and the PWB. Differences between the coefficients of thermal expansion (CTE) of the PWB and the HCC cause severe stresses in the solder joints when the assembly is subjected to large temperature extremes. Methods of resolving the CTE mismatch include using contacts or HCC

sockets, building thick HCC to PWB solder joints to absorb the thermally induced stresses, developing an alternate material with a lower CTE, or reducing the epoxy glass substrate CTE.

Contacts or HCC sockets create an additional electrical interface and require additional real estate. Thick HCC to PWB solder joints do not solve the CTE mismatch, but rather create additional processing problems. Using a low-expansion alternate material, such as Kevlar epoxy (CTE of 5 to 7 ppm/^{o}C), would solve the CTE mismatch; however, material development, difficulty in machining and high water absorption are some of its shortcomings. Reducing the epoxy glass CTE utilizing existing PWB technology and with OSD's patented metal core process results in a PWB compatible with ceramic chip carriers.

2.2 METAL CORE TECHNOLOGY

Epoxy glass has a CTE of 15—20 ppm/ ^{o}C as compared to ceramic having a CTE of 6—7 ppm/ ^{o}C. Reducing the epoxy glass CTE to a value close to 6—7 ppm/^{o}C would result in improved compatibility between the HCC and the PWB. A feasibility study was undertaken, resulting in the decision to investigate metal core technology as a viable HCC substrate interconnection media.

Decreasing the epoxy glass material CTE is accomplished by laminating a low CTE material to the epoxy glass, thereby producing a composite PWB with a CTE closer to that of the HCC ceramic. Initial stress analysis indicated that 0.010 inch thick metal would restrain 0.030 inch thick epoxy glass such that the composite PWB would have a CTE of approximately 8 ppm/ ^{o}C. Sample MLB's were manufactured; and CTE measurements, using a Dupont Model 990 Thermal Analyzer, verified the composite of 0.010 inch thick metal and 0.030 inch thick epoxy glass had a CTE of 8 to 10 ppm/^{o}C.

2.3 EPOXY GLASS/METAL CORE MLB'S — APPROACH AND ACCOMPLISHMENTS

Considering the economics of MLB technology, the maturity of the processes, and the expertise available for design and fabrication of MLB 's, Ordnance Systems elected to solve the device/MLB solder reliability problem. A literature search and Ordnance System tests revealed the failure mechanism of HCC's soldered to epoxy glass MLB's to be solder joint fatique stress. These stresses are due to the different epoxy glass/MLB CTE and ceramic chip carrier CTE.

Utilizing the fact that temperature cycle testing is the best means of thermally stressing the solder joints, OSD evaluated numerous MLB's using the metal core technology. Figure 1 shows these stabilized MLB's. Testing of the metal core technology included in-house IR&D development programs, and an Enhanced Modular

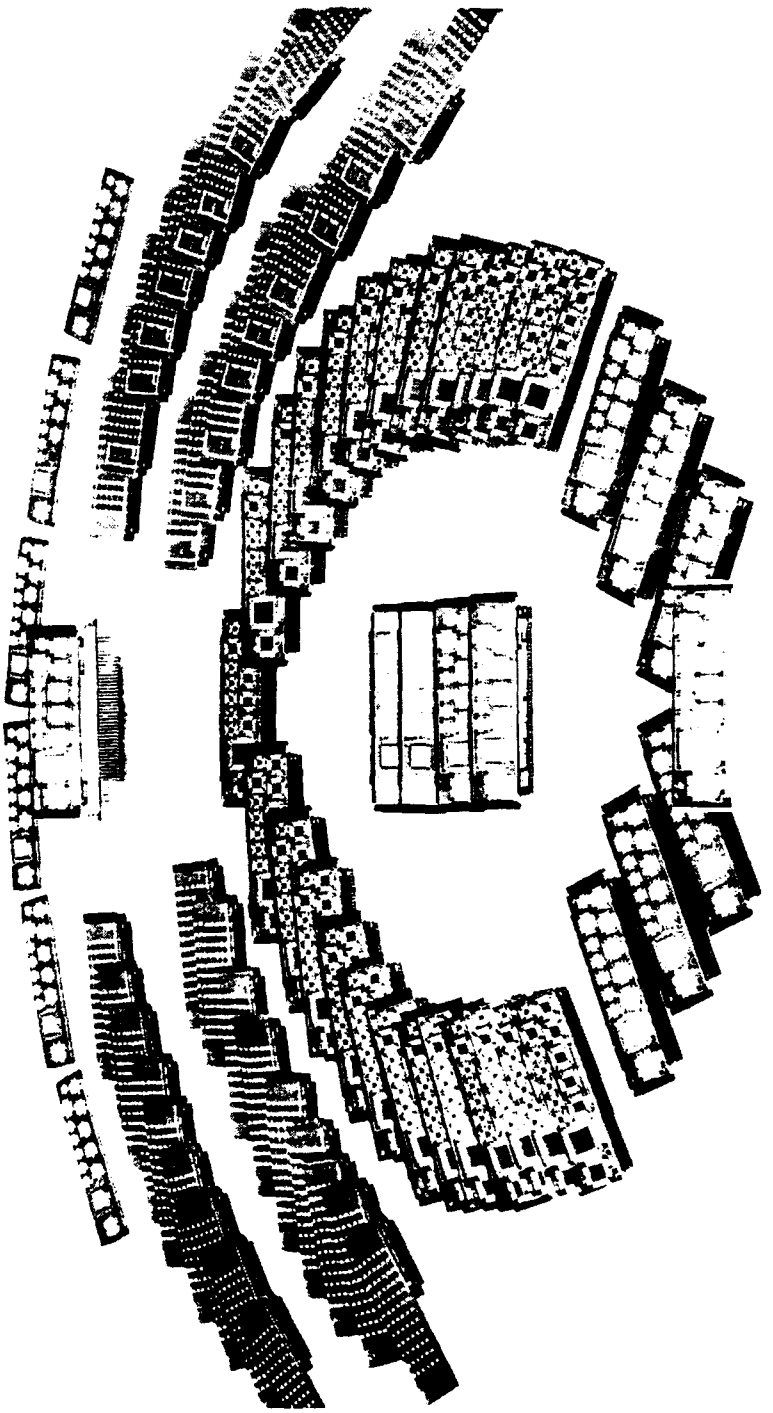


Figure 1. Metal Core Substrate Test Samples

Signal Processor (EMSP) technology assessment proposal. The latter program utilized seven metal core PWB's which were accelerated life tested from −65 ^{o} C to +125 ^{o} C for 600 cycles. The test results of this EMSP program are shown in Figures 2 and 3.

The IR&D program began using six metal core MLB's that were thermally stressed for 500 cycles. Three MLB's, having two layers of 0.003 inch Alloy 42, and three MLB's, having two layers of 0.005 inch Alloy 42, were evaluated (referred to as 0.006 and 0.010, respectively). The 0.006 Alloy 42 samples had 64 lead and 24 lead solder joint failures, but no PTH failures. These solder joint failures may be attributed to not having enough stabilizing material to reduce the MLB composite CTE to a value close to the CTE of the HCC. The 0.010 Alloy 42 MLB's did not encounter solder joint failures, however, excessive PTH failures were encountered. Results of these tests are depicted in Figures 4, 5, and 6.

Micr sections of failed plated-through holes (see Fig. 7a) indicate that the failure mechanism was Z axis expansion. Note also the bulging of the PTH barrel. This clearly indicated that the utilization of two metal layers in place of one thick metal plane would not eliminate the plated-through hole failures.

The metal core plane design was then modified to include nonfunctional pads at each hole location. This would replace the large slug of unsupported expoxy at the hole location with Alloy 42 metal as shown in Figure 7b. Test samples having 0.003 inch and 0.005 inch Alloy 42 were fabricated. This evaluation program has yielded good results, 1,600 cycles with no PTH failures. Testing is continuing and will continue until sufficient number of failures have been observed to permit failure prediction.

Utilization of the metal core layer as a voltage and ground plane is desirable in that it would thus serve two functions and help to minimize the MLB thickness. Preliminary experience with attaching plated-through holes to the metal layer had been successful and evaluation of this connection was initiated.

A special substrate was designed with internal Alloy 42 pads, 0.100 inch x 0.100 inch, interconnected with plated-through holes. Thirty-six substrates were fabricated, eighteen having two 0.003 inch Alloy 42 layers and eighteen having two 0.003 inch Alloy 42 layers and eighteen having 2 oz. copper, and thermal-cycle tested using the same thermal-cycle test as the modules. To date, the samples have survived 2,100 temperature cycles with no failures.

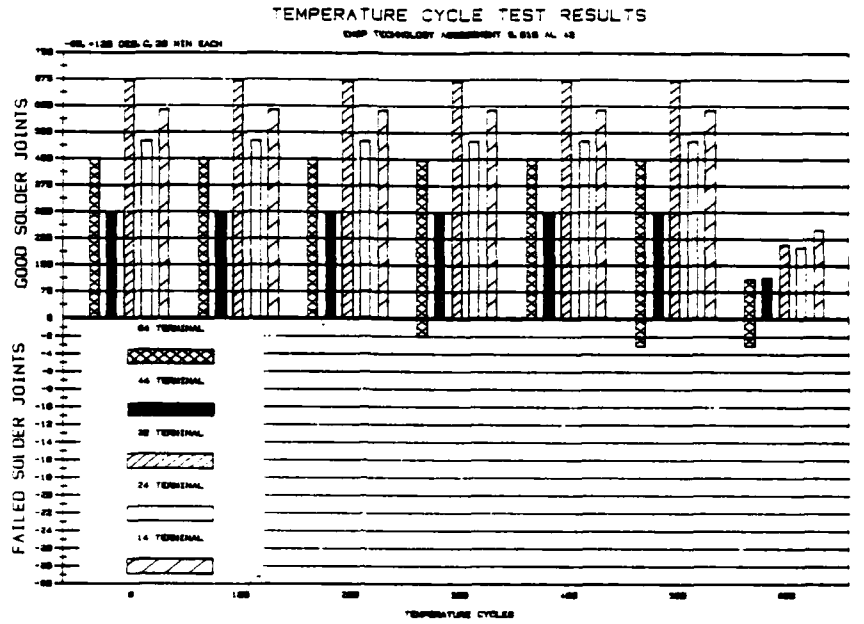


Figure 2. EMSP Temperature Cycle Test Results (Solder Joints)

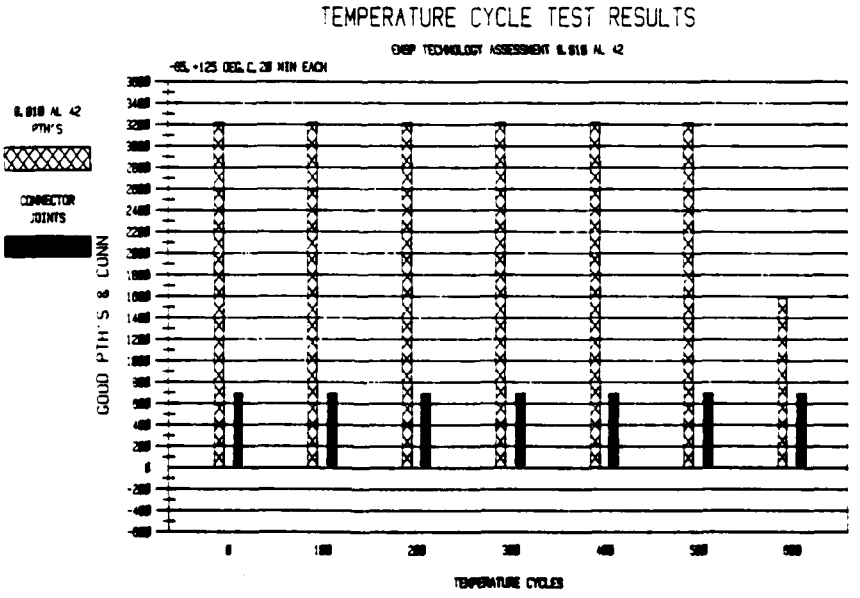


Figure 3. EMSP Temperature Cycle Test Results (Plated-Through Holes & Connector)

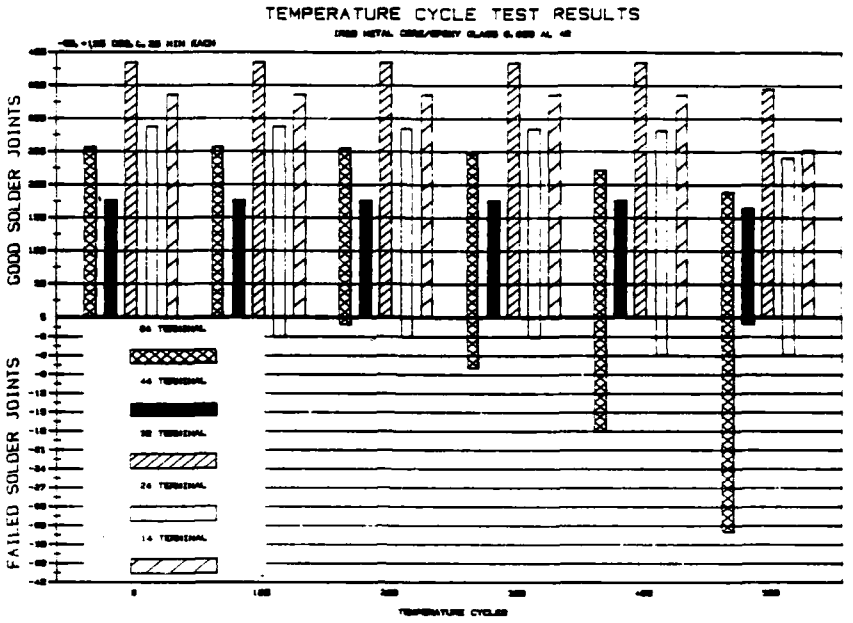


Figure 4. IR&D 0.006 Inch Alloy 42 Temperature Cycle Test Results (Solder Joints)

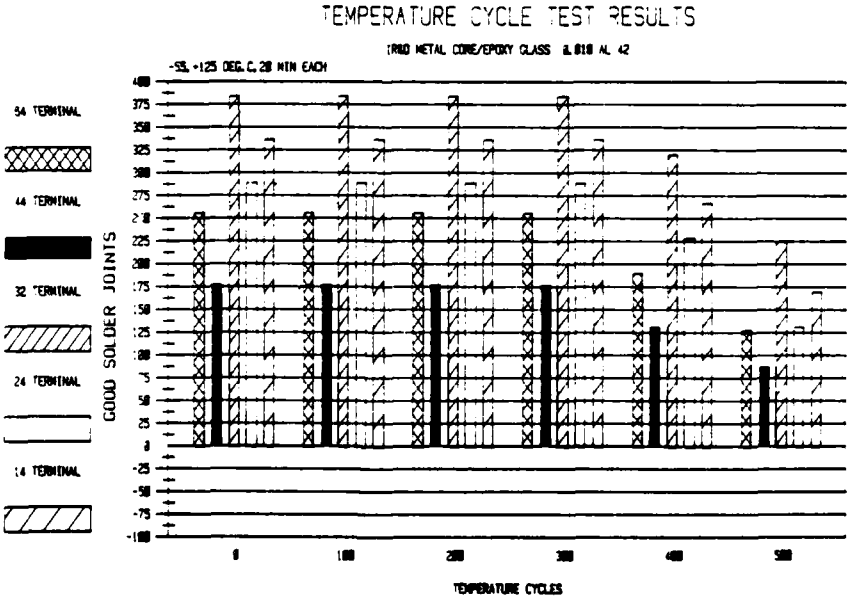


Figure 5. IR&D 0.010 Inch Alloy 42 Temperature Cycle Test Results (Solder Joints)

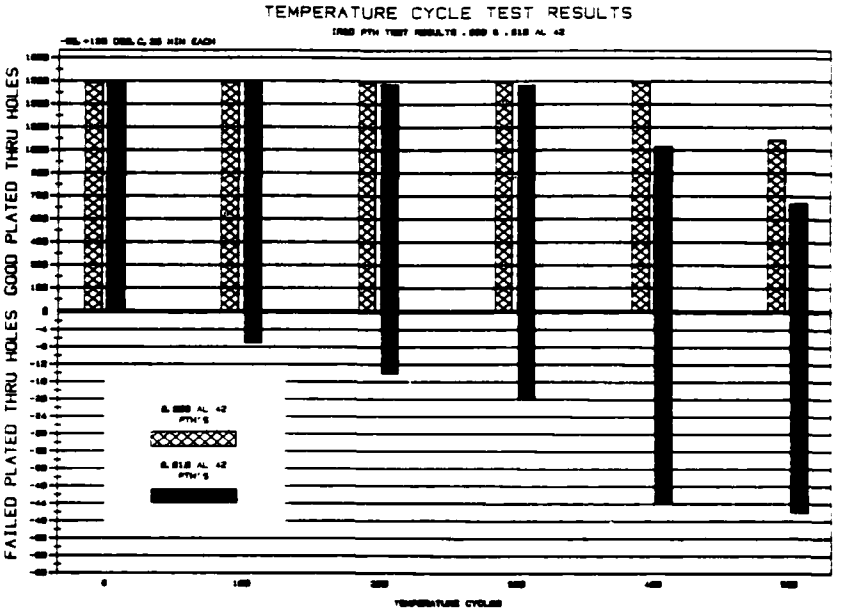


Figure 6. IR&D PTH & Connector Temperature Cycle Test Results (Plated-Through Holes)

a. Without Nonfunctional Pads

b. With Nonfunctional Pads

Figure 7. Failed Plated-Through Hole Microsection

3.0 APPLICABILITY TO NAC

The results from this evaluation program will provide NAC the opportunity to determine the applicability of the newly developed G.E. metal core epoxy glass multilayer board structure to the Standard Electronic Module Format B configuration hardware. Specifically, this program addresses two problems:

a. Ceramic HCC interface to epoxy glass/metal core MLB

b. Epoxy glass/metal core PWB interface to the SEM connector/frame, 0102-710

3.1 TEST PROGRAM

The test program flow chart for the metal core epoxy glass circuit board test program is shown in Figure 8. See Appendix A for explanation of program milestones.

4.0 MLB DESIGN

4.1 MODULE DESIGN

The test module was designed to provide the maximum possible component density utilizing 14, 24, and 32 lead chip carriers and is configured as shown in Figure 9. To minimize PWB construction layup costs, five PWB's were manufactured simultaneously on one precut in a configuration illustrated in Figure 10.

The chip carrier/PWB footprints used in this design were, at the time, the best available. Results from past IR&D accelerated life testing stirred concern on the nonuniformity of these pads. An IR&D program to determine the optimum pad design was in process at the time of the PWB fabrication and, therefore, was not incorporated into the module design. Results of this study are in Appendix B.

The monitoring circuitry for each chip carrier utilizes three separate device continuity circuits and separate connector pin circuits. These three continuity circuits divide the chip carrier footprint into four equal portions which permits locating the open circuit to the nearest chip carrier side. Once the general area of the failure is located, additional continuity testing is performed to specifically locate the open circuit. Test module artwork is shown in Appendix C.

Figure 11 illustrates the chip carrier pad interconnections which are made on successive layers to utilize the PTH's as part of the continuity circuit. Chip carrier input and output runs are fed out to the Type II backplane where each output is wire wrapped to its neighboring chip carrier input, constituting a series loop circuit that is connnected to the GEOS monitor system (described in Section 8.1.2).

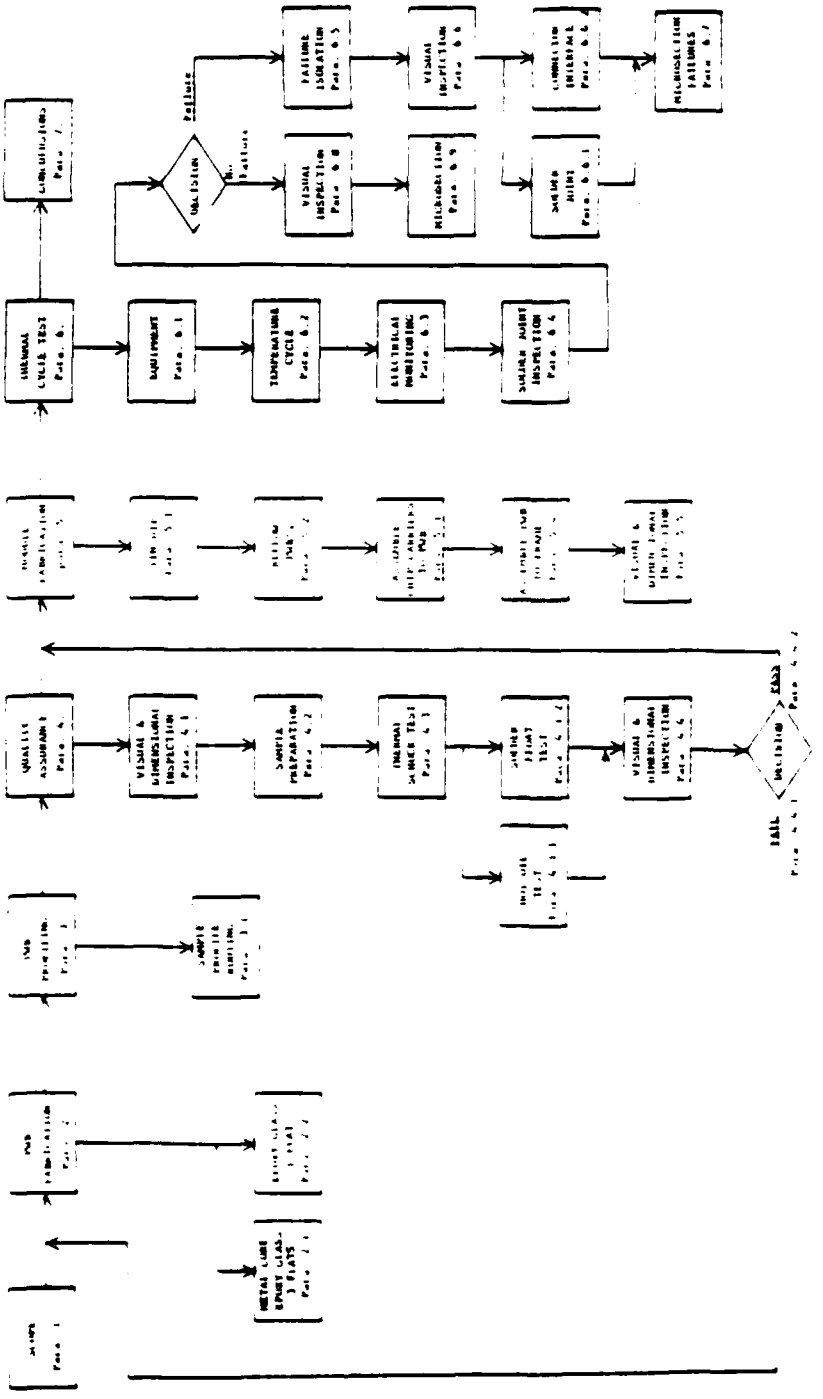


Figure 8. Test Program Milestones

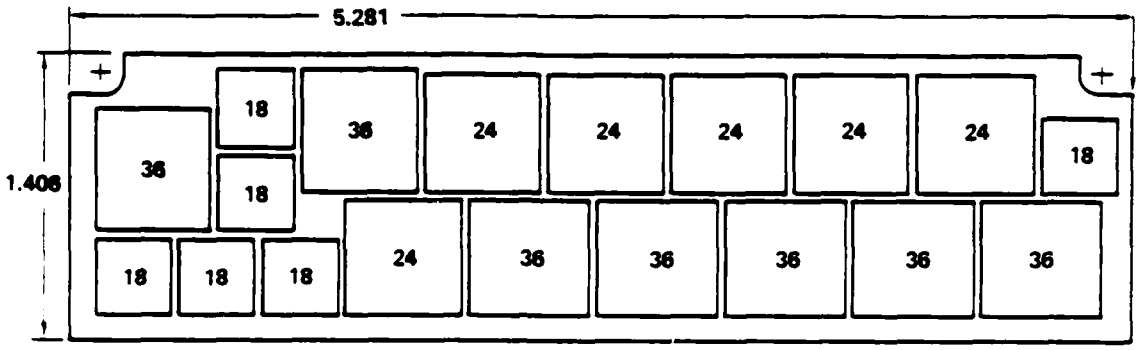


Figure 9. PWB Chip Carrier Configuration

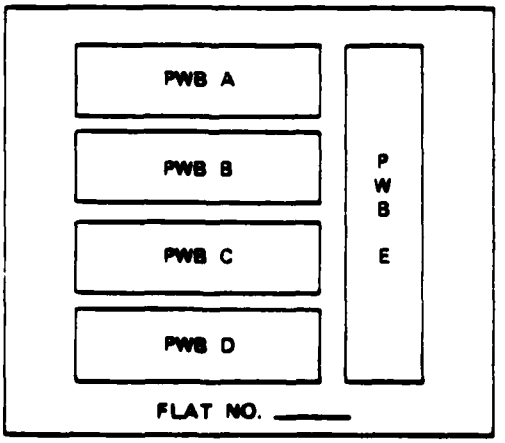


Figure 10. MLB Flat Layout

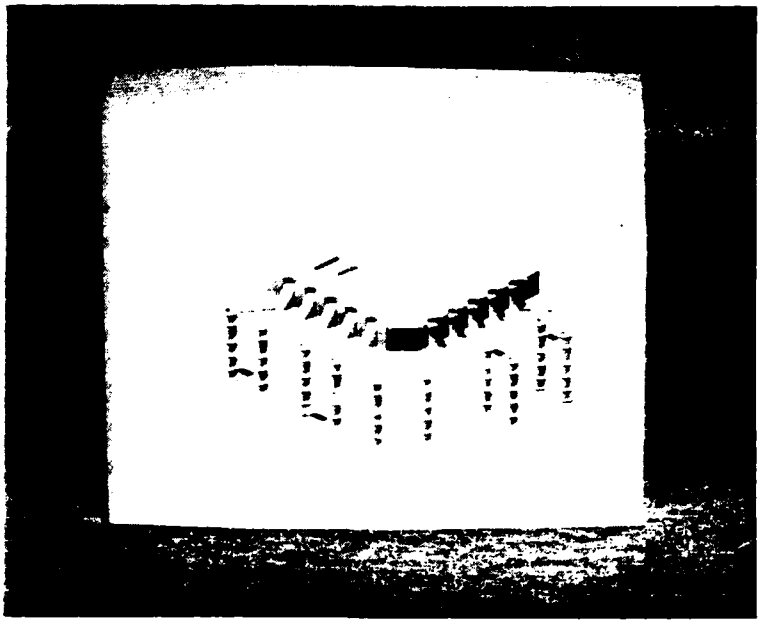


Figure 11. Chip Carrier Pad Interconnection

4.2 CONSTRUCTION LAYUP

The metal core PWB's were fabricated using in-house equipment and GEOS proprietary processes. The .0324 inch thick epoxy glass PWB's were constructed similar to the .0366 inch thick epoxy glass metal core PWB's shown in Figures 12 and 13 respectively, permitting direct comparison of an unstabilized PWB to a CTE controlled PWB.

The metal core and epoxy glass PWB's were profiled to 5.28 x 1.4 inches to fit into the SEM Format B 2A offset Frame 102—710. This connector frame assembly has a one hundred-pin capacity and provides an ample amount of space for chip carrier/ PWB thickness combinations (see Figure 14).

5.0 COMPONENTS

5.1 CHIP CARRIERS

The leadless hermetic chip carriers used in this evaluation program are conventional, cofired multilayer ceramic packages with metal sealing lids which facilitate high packaging density. Figures 15 and 16 show the chip carrier packages that were evaluated and their specification drawing, respectively. Included are 14 lead (.250 x .250 inch), 24 lead (.400 x .400 inch) and 32 lead (.370 x .410 inch) chip carriers, having 0.050, 0.050 and 0.040 inch lead spacing respectively.

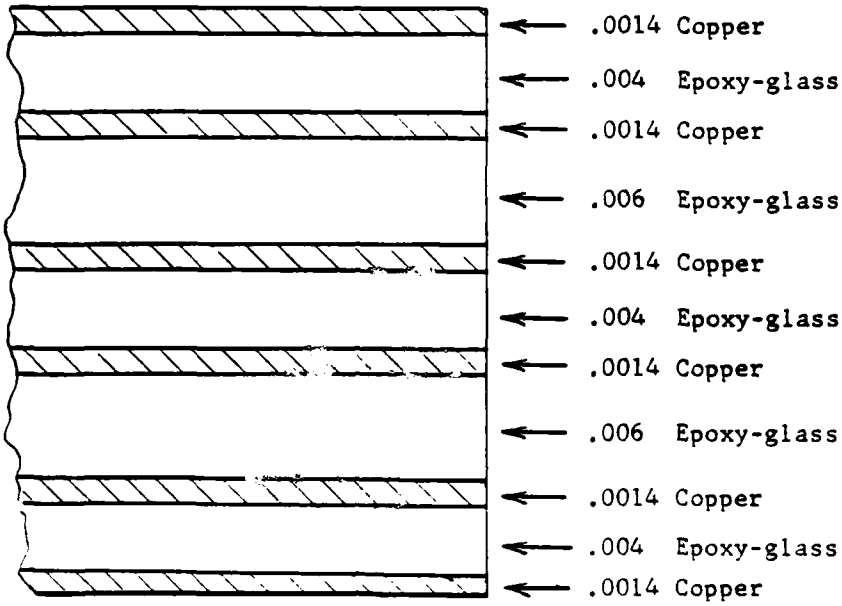


Figure 12. Epoxy Glass Lamination

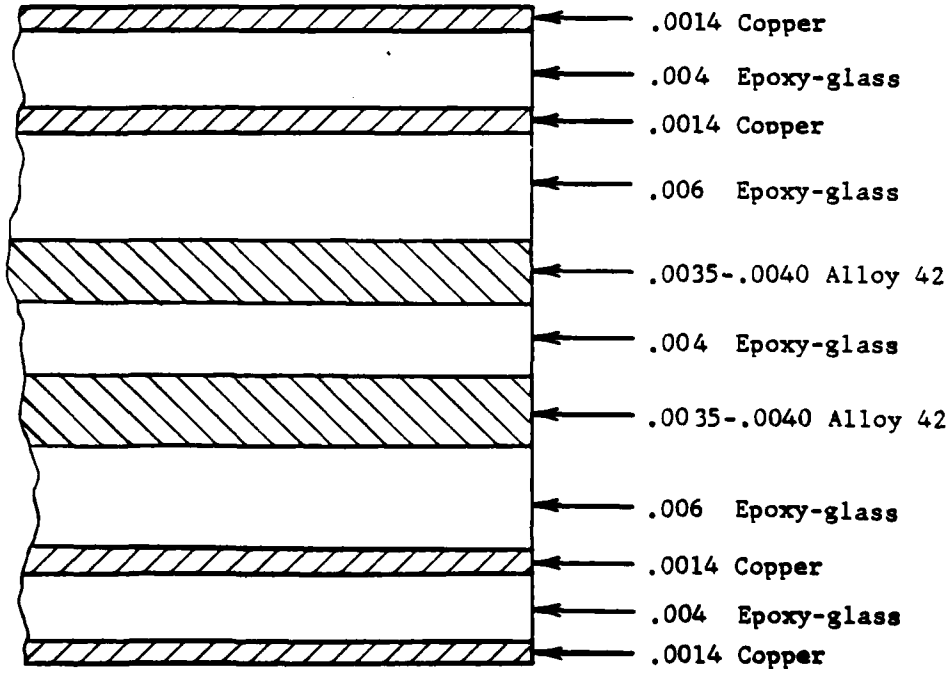


Figure 13. Metal Core/Epoxy Glass MLB Lamination

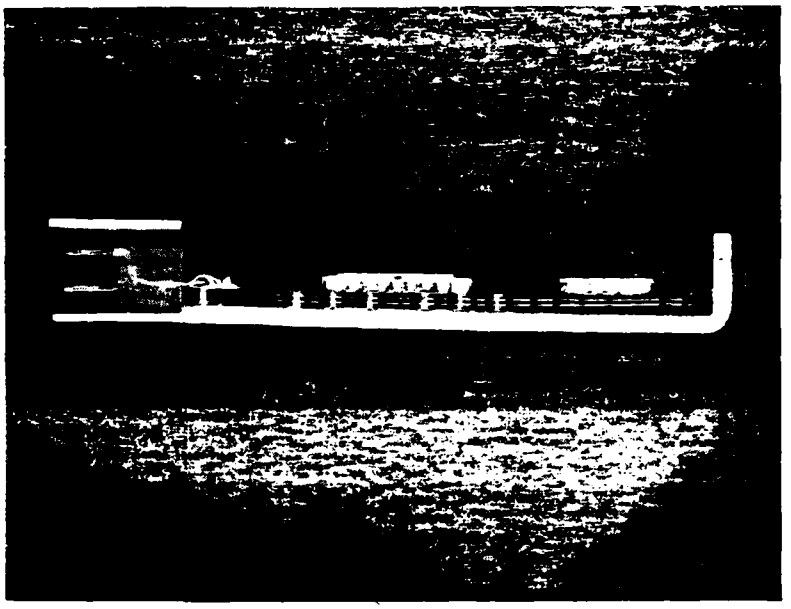


Figure 14. MLB/Frame Assembly

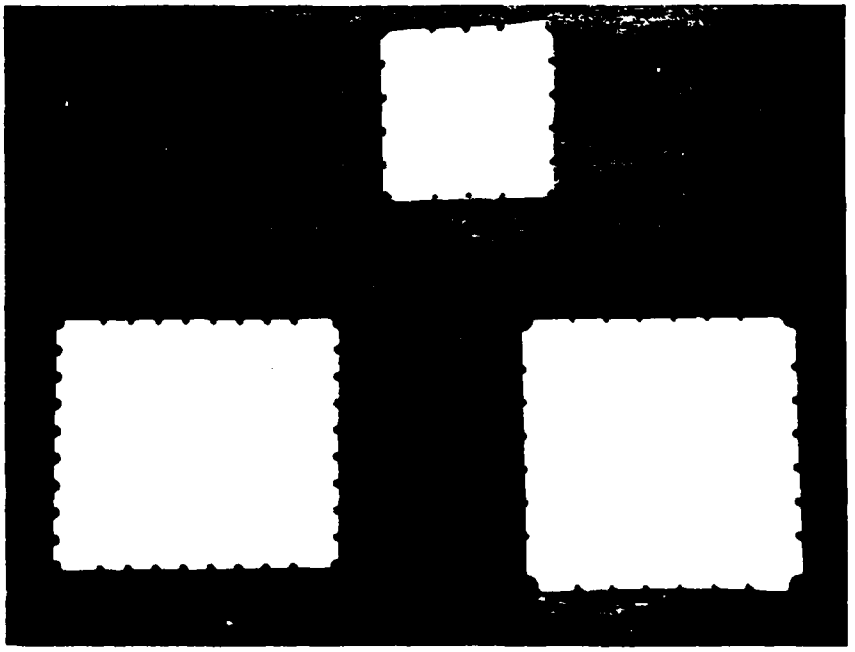


Figure 15. Chip Carriers — Unassembled

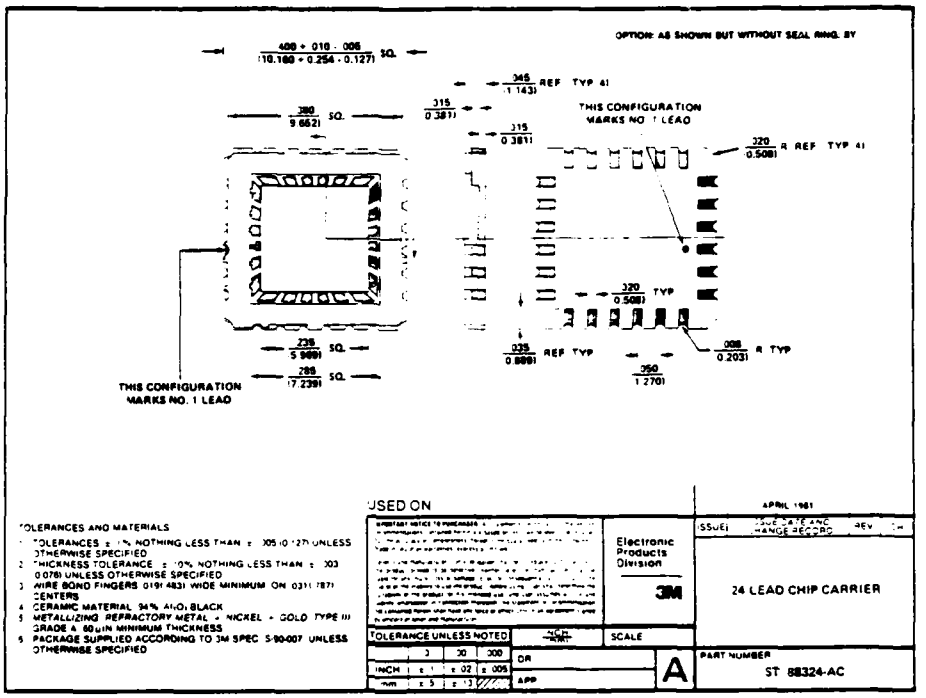


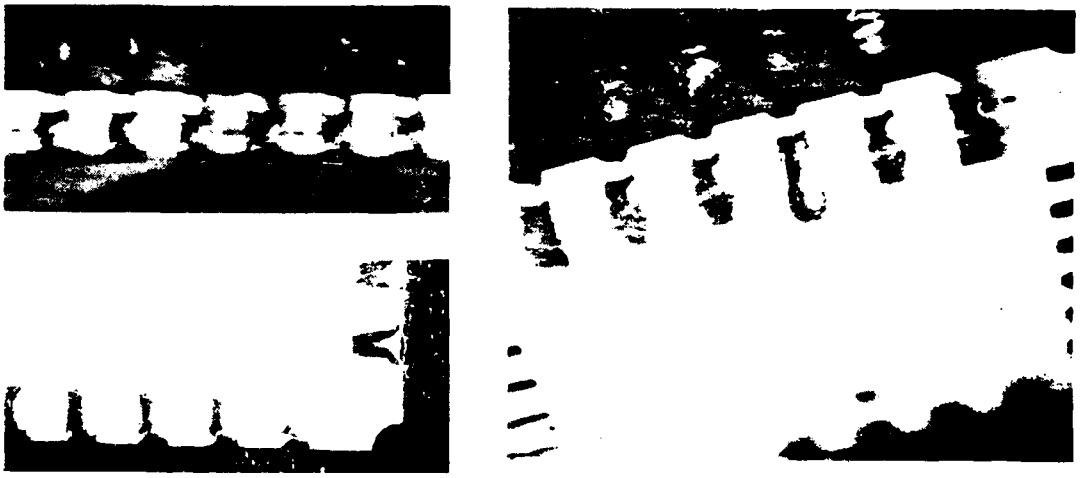
Figure 16. 24 Lead Chip Carrier Specification Drawing

5.2 COMPONENT PREPARATION

To facilitate series loop circuit monitoring, each of the chip carriers had wire bonds installed, connecting pairs of adjacent pads. (The wire bond process uses .001 inch diameter gold wire which forms an interatomic bond between it and the gold HCC pad). To protect the wire bonds and hermetically seal the chip carriers, a gold-plated lid was soldered over the chip carrier cavity using a high temperature solder alloy. This process was performed in nitrogen-purged vessel as a control measure to ensure that contaminants do not affect the HCC performance.

The pads on the underside of the HCC were prepared for assembly to the PWB by pretinning. This ensures that the HCC forms a good solder joint with the PWB's lead-tin solder. The tinning procedure utilized a stainless steel solder pot filled with 63—37 Pb-Sn solder, heated to 220 ^{o} C. The HCC was dipped up to its mid point in flux to ensure all pads were coated. Excess flux was removed from the HCC, and it was floated on the molten solder until the solder wicked up its side terminals. The HCC pads were inspected for uniformity and, where required, refluxing and solder dipping of the nonuniformly tinned chip carriers were performed. The HCC's were cleaned using a vapor degreaser.

Results of this process are as illustrated in Figure 17. Note the volume of solder on each pad. Experience has revealed that all HCC pads must have this amount of solder to ensure a good solder joint will result during component attachment. Experience has demonstrated that too cold a solder pot will result in bridging between the HCC terminals. Too hot a solder pot will result in no build-up of solder on the HCC pads. A typical hermetic chip carrier assembly is shown in Figure 18.



Uniform Tinning

Poor Tinning

Figure 17. Tinned Chip Carriers

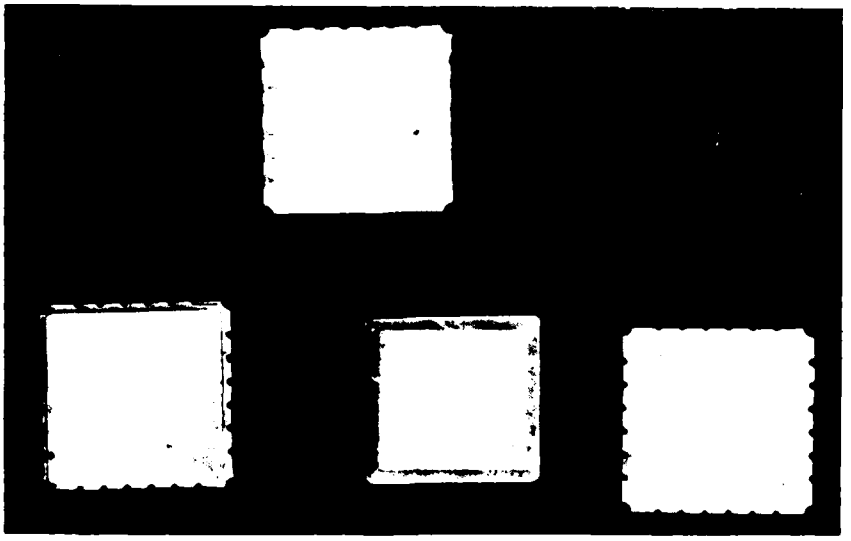


Figure 18. Typical Hermetic Chip Carrier Assembly

6.0 QUALITY ASSURANCE

Reliability of the manufactured PWB's was ensured through a series of quality assurance tests that were performed on test coupons and one PWB per precut. Included in this quality assurance process were visual and dimensional inspections, solder float tests, hot oil dip tests and thermal coefficient of expansion measurements.

6.1 VISUAL AND DIMENSIONAL INSPECTION

The manufacturing test coupon from each precut was inspected and sectioned in compliance with MIL—P—55110C, para. 4.7. The features inspected and their results are outlined below:

1. Plated-through hole and etchback visual examination; all inspection results were within limits of MIL—P—55110C. Figure 19 depicts a microsectioned plated-through hole where the copper and lead-tin plating in the hole is shown continuous and of good quality.

2. Annular ring (external layer), dielectric thickness, undercutting, and conductor overhang dimensional examination; all dimensional results were within limits of MIL—P—55110C. Table 1 shows the Military Specification requirement and measured results of dimensional examinations. See Figure 20 for plated-through hole microsection.

3. Metal core stabilizing layer termination point delamination inspection; as shown in Figure 21, no delamination occurred.

6.2 SOLDER FLOAT

A thermal stress solder float test in accordance with MIL—P—55110C, para. 4.8.7, was performed on one half of one PWB from each precut. Examination of PTH microsections showed no PTH integrity problems. See Figure 22.

6.3 HOT OIL DIP

Although MIL—P—55640A has been superseded by MIL—P—55110C, a hot oil dip in 260°C oil was performed on the remaining half of the solder float test samples. Figure 23 dipicts the results of this test and shows good PTH integrity and no delamination.

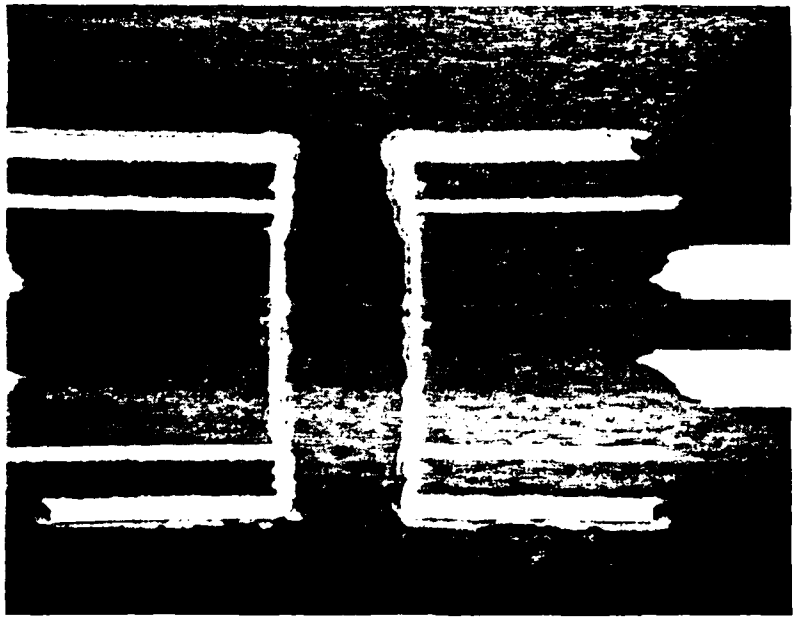


Figure 19. Plated-Through Hole Photomicrograph — Visual Inspection

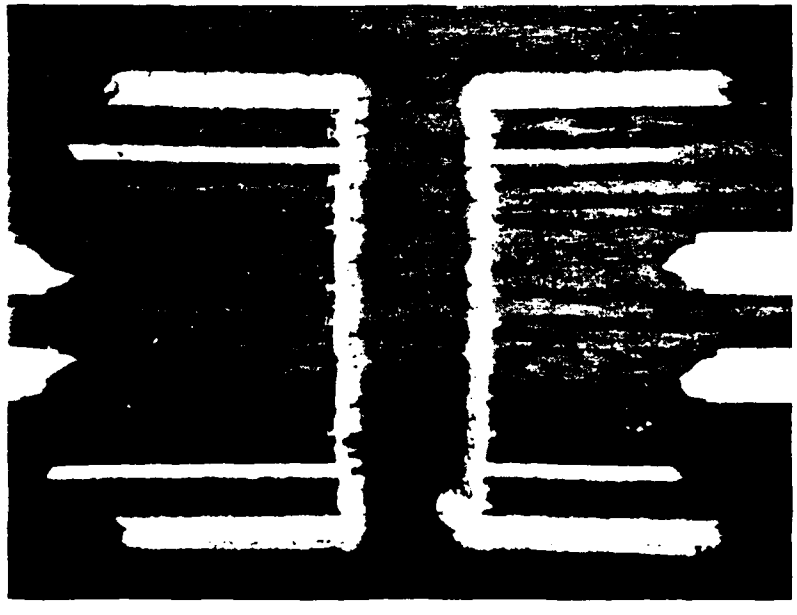


Figure 20. Plated-Through Hole Photomicrograph — Dimensional Inspection

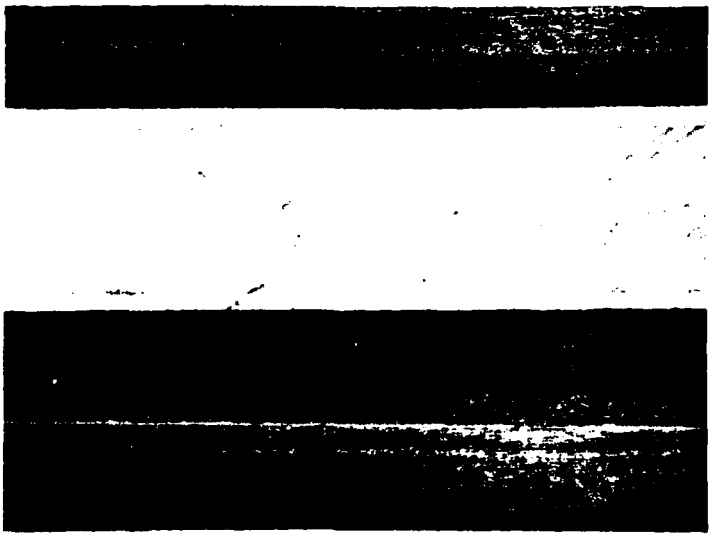


Figure 21. Plated-Through Hole Photomicrograph — Metal Core Inspection

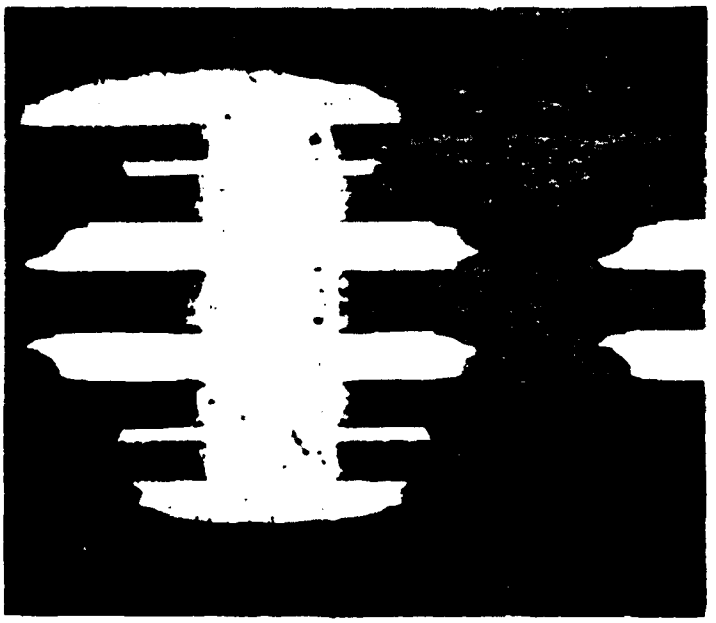


Figure 22. Quality Assurance Stress Test — Solder Float

Table 1.

VISUAL AND DIMENSIONAL INSPECTION

DESCRIPTION	SPEC. REQUIREMENTS (INCHES)	MEASURED (INCHES)
ANNULAR RING (EXTERNAL)	MIN. OF 0.005 ONE SIDE 0.004 ON THE OTHER	0.0061 MIN
DIELECTRIC THICKNESS	MIN. OF 0.0035	0.0045 MIN
UNDERCUTTING	LESS THAN 0.0024	0.0018 MAX
CONDUCTOR OVERHANG	NO OVERHANG	NO OVERHANG
COPPER PLATING	0.001 MIN.	0.0014 MIN
LEAD-TIN PLATING	0.0003 MIN.	0.00046 MIN
MISREGISTRATION	0.014 MAX	0.008 MAX

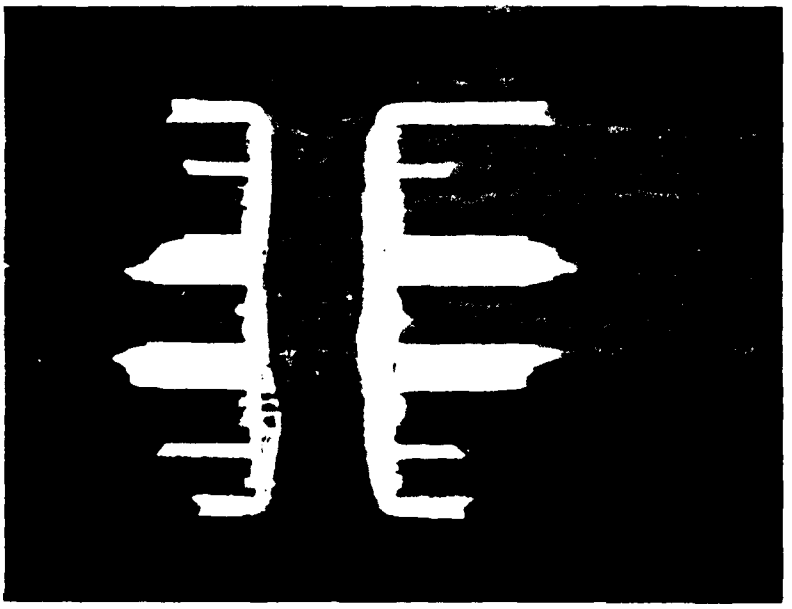


Figure 23. Quality Assurance Stress Test — Hot Oil Dip

6.4 COEFFICIENT THERMAL OF EXPANSION TESTS

Coefficient thermal of expansion tests were performed on two metal core PWB's and one epoxy glass PWB to determine the expansion of the conventional epoxy glass and the effectiveness of the metal core layers in the stabilized PWB's. Both "X" and "Y" direction measurements were performed to determine what impact the direction of the glass cloth weave has on the PWB's CTE as illustrated in Figure 24.

A strain gage measurement method was developed which compares the test sample expansion to that of a stable reference material such as Titanium Silicate. The CTE was determined by Δ microstrain/ Δ temperature + CTE_{ref} = slope of line + CTE_{ref}. The slope was determined by the use of a computer program which produces an equation that best fits the points in the least-squares sense for each CTE linear plot. Tabulated CTE results and material thicknesses are shown in Table 2.

In Figure 25, the CTE of the non stabilized epoxy glass MLB is 17.8 ppm/^{o}C in both the X and Y directions. Since the CTE is the same for the X and Y direction, the prepreg's glass cloth weave may be assumed to have been alternated during lamination. Figure 26 shows the CTE curve for precut 90, which has two 0.005 inch Alloy 42 layers. The lower CTE in the X direction implies that the prepreg's glass weave "grain" is in the X direction. Conversely, Precut 91, Figure 27, has the glass weave "grain" in the Y direction which causes a higher expansion in the X direction. Because the difference in the X and Y CTE's of Precuts 90 and 91 is not substantial, the grain direction of the glass weave did not influence solder joint failures on one side of the HCC (X) more than its other side (Y).

7.0 MODULE FABRICATION

Evaluation of any HCC interconnection substrate materal is dependent on the assembly of the HCC to the substrate. To optimize this process, IR&D effort was expended to develop a component assembly process which results in HCC's having all terminals soldered to the footprint pads with good solder fillets.

7.1 SOLDER PROCESS INVESTIGATION

7.1.1 CONDUCTIVE SOLDER PROCESS

Initially, IR&D metal core chip carrier PWB's were designed to accommondate 18, 24, and 36 pad HCC's and interface with the Standard Electronic Module 1A frame and forty-pin connector. The HCC's for this assembly were soldered to the PWB's utilizing a two-zone Browne conveyer solder reflow machine with nitrogen forming gas. Flux was not used for this operation and, therefore, no cleaning was required.

Table 2.

MATERIAL DESCRIPTION	MATERIAL THICKNESS (INCHES)		CTE (PPM/DEG C) X	Y
2 LAYERS OF 2 OZ COPPER PRECUT 94	EPOXY GLASS COPPER PLANE	0.0251 0.0056	17.8	17.8
2 LAYERS OF 0.005 AL 42 PRECUT 90	EPOXY GLASS ALLOY 42 INTERNAL COPPER PLATE	0.0329 0.0098 0.0027	8.58	9.4
2 LAYERS OF 0.005 AL 42 PRECUT 91	EPOXY GLASS ALLOY 42 INTERNAL COPPER PLATE	0.0323 0.0099 0.0026	9.33	8.4

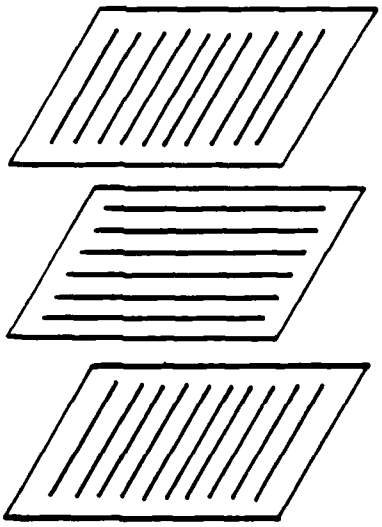


Figure 24. Glass Cloth Weave Grain Direction of Epoxy Glass Prepreg

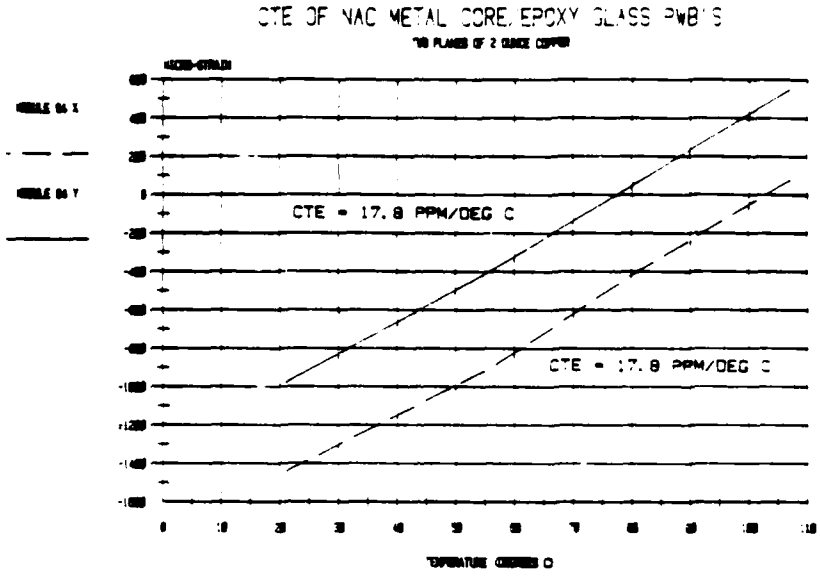


Figure 25. Coefficient of Thermal Expansion — 2 Planes of 2 oz. Copper (Precut 94)

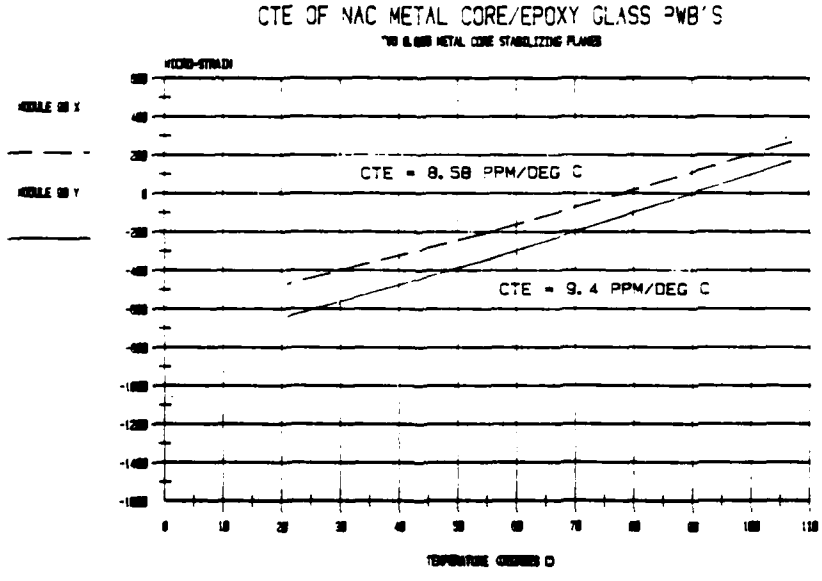


Figure 26. Coefficient of Thermal Expansion — 2 Planes of 0.005 Alloy 42 (Precut 90)

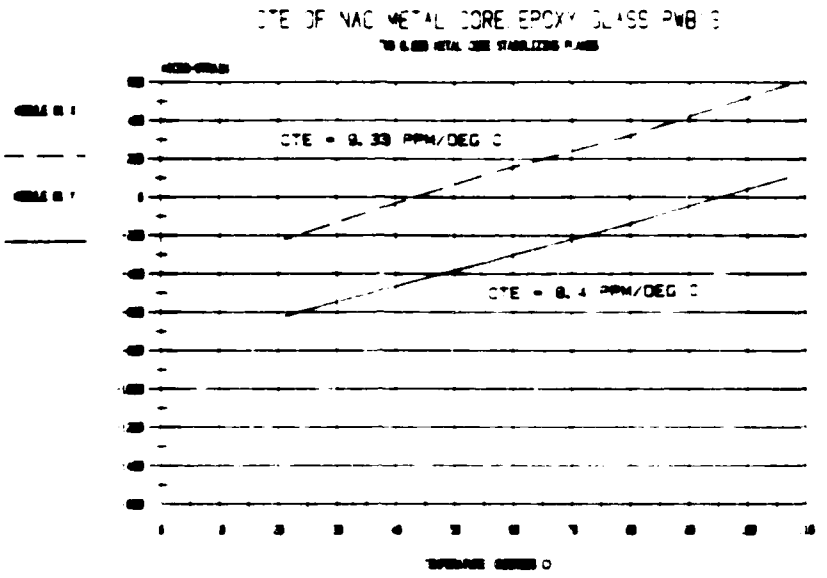


Figure 27. Coefficient of Thermal Expansion — 2 Planes of 0.005 Alloy 42 (Precut 91)

This process provided excellent results for soldering 14, 24 and 36 terminal divides to the 1.0" x 2.2" PWB's used in Standard Electronic Modules (SEM 1A). The impact of PWB warpage is minimized by the small size of the MLB and chip carriers.

One drawback of the conduction reflow process is that the reflow temperature must be 270 °C which casues charring of the MLB. Warpage, due to the large temperature gradient induced in the MLB, inhibits complete component reflow to the ISEM 2A PWB's in spite of the symmetrical PWB layup. Therefore, this conduction reflow process was not recommended for this metal core epoxy glass PWB chip carrier evaluation program.

7.1.2 HOT OIL SOLDER PROCESS

The hot oil solder process consists of using a silicone oil (SF1154) or peanut oil reflow medium heated to 220 °C to 230 °C. The PWB assembly is fluxed and pre-heated to approximately 150°C, then lowered into the hot oil.

An assembly fixture is used to align the chip carriers and hold them in place over the chip carrier footprints. Figure 28 shows an assembled MLB, its line-up fixture, and the MLB prior to component assembly.

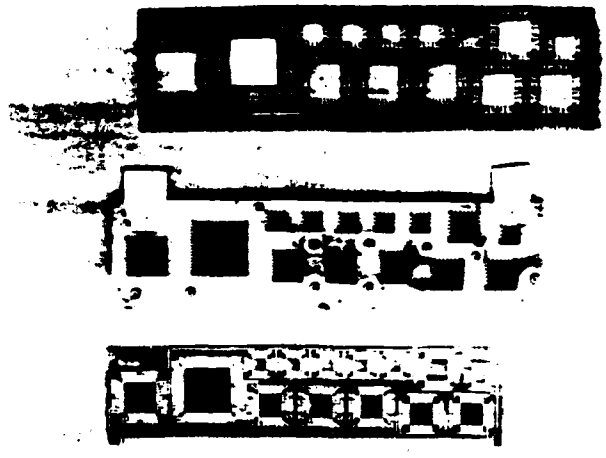


Figure 28. HCC Assembly Fixture

Removal of several HCC's from assembled IR&D PWB's revealed a clean PWB with no visible trace of flux residue. The nature of the flux removal is not completely understood at this time, but one theory is that the flux is boiled from the PWB when it is first immersed into the hot oil bath.

PWB warpage is significantly reduced with this process because of uniform heating from the efficient heat transfer of the oil to the PWB's. This means less time is required for reflow which is better for the PWB and its components.

Because of difficulty in cleaning the silicone oil from the assembled PWB and the faster heating rate of the vapor phase relfow system, the vapor phase solder process was investigated.

7.1.3 VAPOR PHASE SOLDER PROCESS

The vapor phase solder reflow process utilizes the storage of potential energy in the form of vapor to change phase to liquid during condensation. This phenomonon is known as latent heat of vaporization, and it is the most efficient method of heat transfer for solder reflow known today.

Figure 29 shows the HTC model 912 vapor phase solder machine which utilizes two vapor regions, one that has a high boiling temperature (primary, 215°C) to reflow the solder, and one with lower boiling temperature (secondary) to act as a blanket to minimize drag-out of the primary vapor. A filtering system is incorporated on the vapor phase machine to remove the solid suspension of flux residue obtained during reflow.

7.2 MODULE ASSEMBLY

The vapor phase reflow process was utilized to reflow the HCC's to the PWB's. A fifteen-second reflow time was used for the twelve metal core and four epoxy glass PWB's. Diluted flux was applied to the chip carrier—PWB interface, and an alignment fixture was utilized to aid in positioning the chip carrier over the footprints during reflow. See Figure 28.

Each PWB was cleaned after reflow by immersing it in a vapor degreaser and using its sprayer to remove any residual flux from under the chip carrier.

7.3 INSPECTION AND TOUCH-UP

Each chip carrier solder joint was inspected utilizing a 20X microscope for determining solder joint fillet qualities. Each fillet was inspected for: (1) connection between the chip carrier and PWB footprint, (2) shiny appearance, and (3) smooth, full fillets. 99.3% of the solder joints met the good fillet criteria, while the remaining .7% required touch-up with a fine-tipped, temperature-controlled soldering iron and the addition of flux. A second cleaning in a vapor degreaser was followed by reinspection of the touched-up fillets.

7.4 PWB-FRAME ATTACHMENT

The assembled chip carrier PWB was attached to the SEM Format B 2A offset frame with RTV silicone adhesive. The adhesive was applied .004 to .006 inches thick to the non-component side of the MLB and inserted into the module frame. Pressure was applied to the frame—PWB interface to ensure complete bonding. The connector terminals were soldered to the MLB using a fine-tipped, temperature-controlled soldering iron and, where warranted, the addition of 63/37 Pb-Sn solder.

8.0 ACCELERATED LIFE TESTING

Temperature cycle testing has been established as the best means for thermal stressing the solder joints. This testing was comprised of automatically moving the modules from a high-temperature chamber, +125°C, to a low-temperature chamber, −55°C, dwelling at each extreme for 20 minutes. The time/temperature curve for module temperature response is depicted in Figure 30.

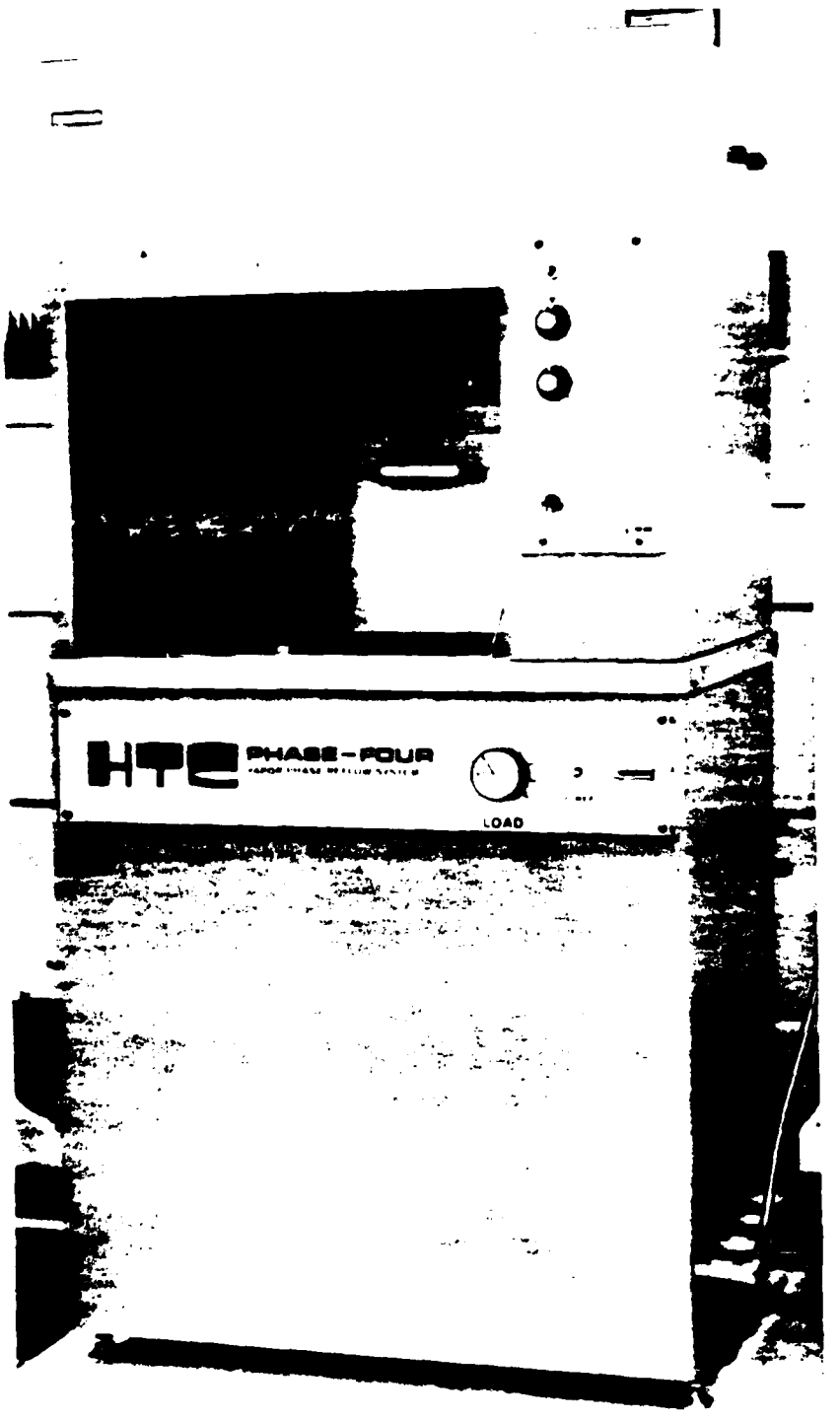


Figure 29. HTC Model 912 Vapor Phase Reflow Machine

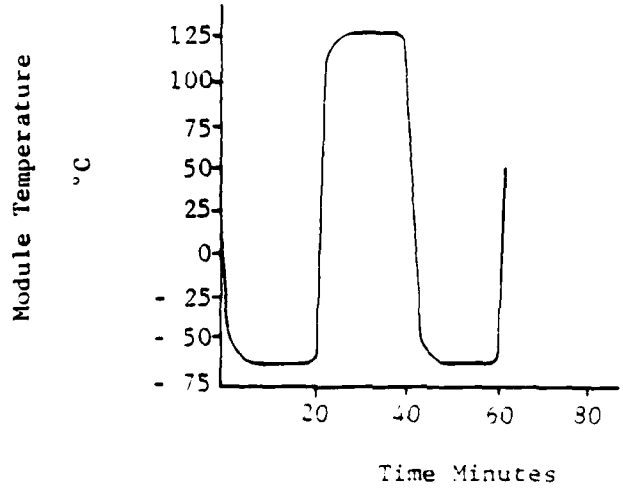


Figure 30. Module Temperature Response

8.1 EQUIPMENT

8.1.1 RANSCO THERMAL CHAMBER

A Ransco 7107−1 thermal shock chamber with 6 kilowatt heating and 15 horsepower cascade refrigeration was utilized for the accelerated life testing. This thermal shock chamber has an elevator that moves between the high temperature cavity (+125 ^{o} C) and the low temperature cavity (−55 ^{o} C), yielding very quick temperature extreme changes resulting in thermally shocked, chip carrier modules. See Figure 31.

8.1.2 GEOS CONTINUITY MONITOR

Test samples were electrically monitored to detect an open circuit using a 14 station GEOS continuity tester shown in Figure 32. This monitoring equipment indicates which PWB failed and at what cycle number that particular PWB failed. If the resistance of the PWB−chip carrier circuit goes above approximately 10K ohms, a light appears on the monitor indicating an open circuit has occurred. A pulse counter is incorporated into the monitor to identify the cycle number at which the particular open occurred.

8.2 TEST RESULTS

8.2.1 EPOXY GLASS SOLDER JOINTS

Temperature cycle test results of solder joints and PTH's are depicted in Figures 33 and 34 respectively, for samples constructed with epoxy glass having chip carriers directly mounted to them.

Under thermal cycling conditions (—55 °C to 125 °C, 20 minute dwell) the epoxy glass MLB's had early failures. Approximately 60% of the solder joints were cracked and registered as open circuits at 100 cycles. At 200 cycles, the failure rate was up to nearly 75%.

Figure 35 depicts one of the many failed solder joints encountered on the epoxy glass MLB's after 200 thermal cycles. As the crack propagated from under the chip carrier to the solder fillet, it continued through the fillet at the smallest cross section (occuring perpendicular to the outer surface of the fillet). Readily noticeable is the flat shearing of the solder under the chip carrier. This shearing was caused by the large difference in CTE's between the epoxy glass, 17.8 ppm/ °C, and the chip carrier ceramic, 6.8 ppm/ °C. The benefit of having a full solder fillet is seen here.

The coefficient of thermal expansion of a material represents the change in length, per unit length, per degree of temperature. As the size of an object increases, the impact of the CTE increases and, consequently, the greater it will expand under thermal changes. Similarly, the greater the thermal gradient a chip carrier (CTE of 6.8 ppm/ °C) and substrate (CTE of 17.8 ppm/ °C) is subjected to, the more the substrate will expand compared to the chip carrier and, therefore, induce stresses. For example, if the chip carrier and substrate are subjected to a temperature differential of —55 °C to +125 °C, the expansion of the chip carrier and substrate would be:

$$\Delta T = +125 - (-55) = 180^{\circ}C \quad (1)$$

24 terminal chip carriers (.4 x .4 in),CTE of 6.8×10^{-6} in./in./°C.

$$6.8 \times 10^{-6} \text{ in./in./}^{\circ}C \times 180^{\circ}C = 1.224 \times 10^{-3} \text{ in./ in. x .4 inch} = .489 \times 10^{-3} \text{ inch.} \quad (2)$$

Epoxy glass footprint size (.4 x .4 in),CTE of 17.8×10^{-6} in./in./°C

$$17.8 \times 10^{-6} \text{ in./in/}^{\circ}C \times 180^{\circ}C = 3.204 \times 10^{-3} \text{ in./in. x .4 in.} = 1.28 \times 10^{-3} \text{ inch.} \quad (3)$$

Δ Expansion = epoxy glass expansion — chip carrier expansion

$$1.28 \times 10^{-3} \text{ in.} - .489 \times 10^{-3} \text{ in.} = .792 \times 10^{-3} \text{ inch.} \quad (4)$$

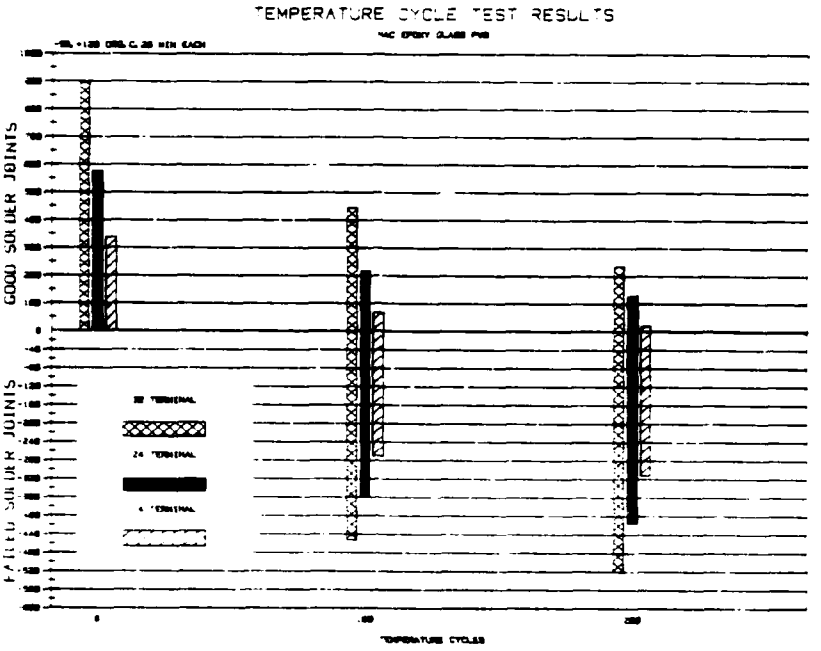


Figure 33. Epoxy Glass Temperature Cycle Test Results (Solder Joints)

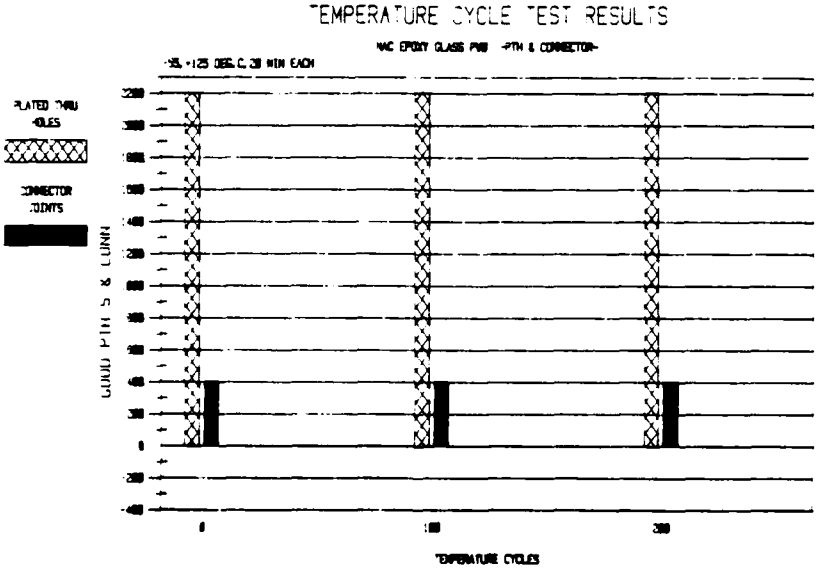


Figure 34. Epoxy Glass Temperature Cycle Test Results
(Plated-Through Holes & Connector Joints)

Figure 35. Failed Solder Joint

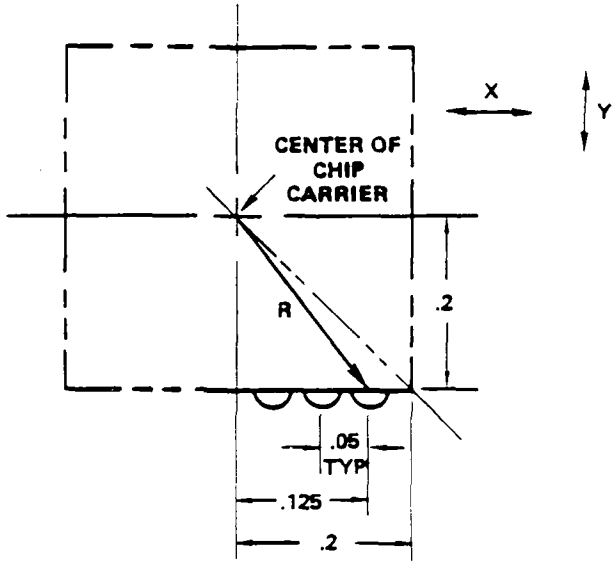
Assuming that the center of the chip carrier does not move relative to the center of the substrate footprint, because of symmetry, and only considering one-eighth of the chip carrier, the outermost solder joints will be subjected to half the expansion of the overall chip carrier.

$$\frac{.792 \times 10^{-3}}{2} = .396 \times 10^{-3} \text{inch} \quad (5)$$

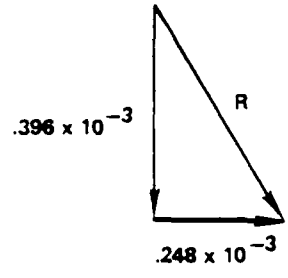
In the X direction, the expansion will be:

$$\frac{.125 \times .396}{.2} = 2.48 \times 10^{-6} \text{inch} \quad (6)$$

The Y direction expansion will be simply $.396 \times 10^{-3}$ inch.



The resultant movement of the chip carrier solder joint relative to its center becomes:



$$R = \sqrt{(.396 \times 10^{-3})^2 + (.248 \times 10^{-3})^2}$$

$R = .467 \times 10^{-3}$ inches radially from the chip carrier's center. (7)

The end solder joint must restrain this movement of $.467 \times 10^{-3}$ inches while the second and third solder joints must restrain $.423 \times 10^{-3}$ and $.399 \times 10^{-3}$ inches of motion respectively, under the conditions of thermal cycling. The stresses caused by the substrate being restrained by the HCC and solder joints, causes the solder joints to fatigue and ultimately fail.

When evaluating the different size chip carriers and their pad locations, two variables are encountered. First, the end solder joints on the chip carrier would see the most stress and should, therefore, fail first. Second, the larger the chip carrier, the earlier the failures are expected to start. These generalizations are true only if the chip carrier pads protruding from the chip carrier are of uniform lengths and widths, and the volume of the solder on those pads are equal.

The 32 terminal chip carriers (.040 terminal spacing) encountered more failures than the 24 terminal chip carriers (.050 terminal spacing) because the width of the solder joint pads were less. The .020 inch wide metalization of the 32 terminal chip carrier, as compared to the .025 inch wide metalization of the 24 terminal chip carrier, are 20% smaller and were, therefore, expected to fail earlier.

Due to the rapid failure rate of the HCC solder joints encountered at 100 cycles on the epoxy glass—chip carrier modules, it was not possible to observe which HCC device type (32, 24 or 14 terminal) failed first. This is the main reason why the temperature cycle test results of the epoxy glass MLB's do not coincide with the metal core temperature cycle test results.

The early failures encountered on the epoxy glass MLB's are attributed to the large mismatch in thermal expansion between the epoxy glass (17.8 ppm/ ^{o}C) and the ceramic chip carrier (6.8 ppm/ ^{o}C). Interpreting these results indicates that using chip carriers directly mounted on conventional epoxy glass PWB's is not an acceptable means of interconnection.

8.2.2 PLATED-THROUGH HOLES AND CONNECTOR JOINTS — EPOXY GLASS

No failures were encountered regarding PTH's and connector joints on the epoxy glass MLB's because of the low number of cycles completed. A typical connector solder joint is shown in Figure 36. Note the large contact area between the soldered connector tab and the PWB pad.

8.2.3 METAL CORE EPOXY GLASS SOLDER JOINTS

Figures 37 and 38 show the temperature cycle test results for the metal core epoxy glass stabilized MLB's with chip carriers mounted directly to them.

During temperature cycling (—55 ^{o}C to +125 ^{o}C, 20 minute dwell), the first three failures were encountered at 400 cycles on the 24 terminal HCC's. The 32 lead HCC's had five failures at 500 cycles, with the 14 terminal HCC's not encountering any failures until 600 cycles. The percent of solder joint failures for the 32, 24 and 14 terminal HCC's are listed in Table 3.

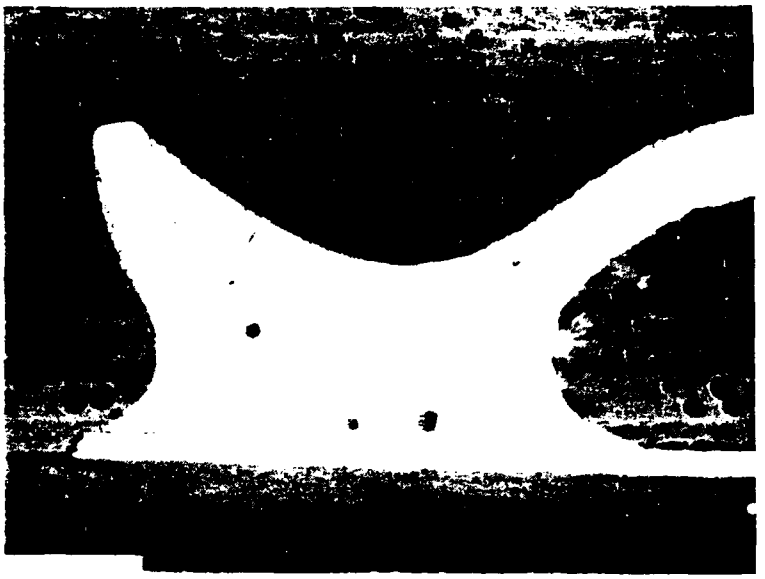


Figure 36. Good Connector Solder Joint

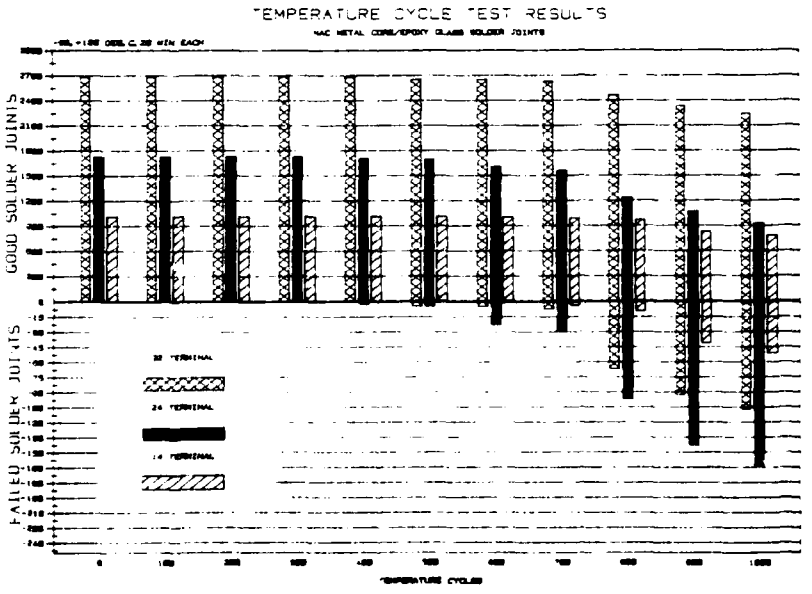


Figure 37. Metal Core Epoxy Glass Temperature Cycle Test Results (Solder Joints)

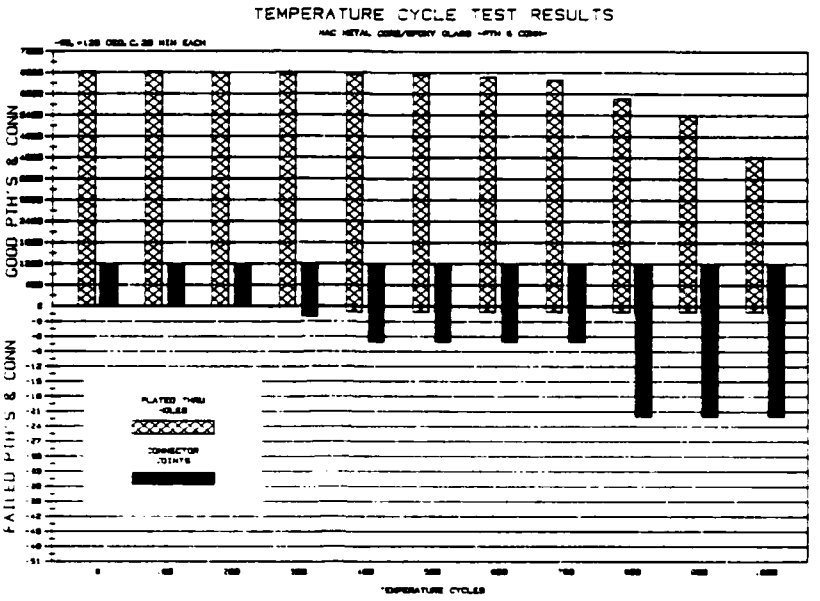


Figure 38. Metal Core Epoxy Glass Temperature Cycle Test Results (Plated-Through Hole and Connector Solder Joints)

Table 3.

NAC METAL CORE EPOXY GLASS SOLDER JOINTS PERCENT FAILURES OF SOLDER JOINTS			
CYCLES	32 LEAD	24 LEAD	14 LEAD
100	0	0	0
200	0	0	0
300	0	0	0
400	0	0.12	0
500	0.14	0.23	0
600	0.14	1.35	0.01
700	0.26	1.86	0.30
800	2.55	6.19	0.91
900	3.73	11.60	4.24
1000	4.59	15.28	6.20

Because of the high number of failures encountered with the 24 terminal HCC's, the location of the failures relative to the pad geometry was investigated. Readily noticeable in Figure 39 are the nonuniform pad shapes on the 24 terminal HCC. The two center pads are very short and do not protrude from the HCC far enough to obtain a full fillet. The four remaining pads, on the other hand, are long and protrude from the HCC more than what is desirable.

A chart of the short pad failures and the long pad failures was generated (Figure 40) in order to clarify the 24 terminal HCC failure phenomenon. As pointed out in Section 8.2.1, equation 7, the movement of the substrate relative to the HCC is a function of the distance from the center of the HCC to the solder joints. The farther the solder joint is from the center of the HCC, the more the movement will be encountered, resulting in a larger stress induced in the solder joints. Conversely, solder pads closer to the center of the HCC will experience smaller stresses. Applying this theory to the 24 terminal HCC pads reveals that since the short center pads experienced less stress but failed at nearly the same rate as the long end pads, the short pads are of poor design and should protrude farther from the HCC similar to those in Figure 41.

The solder joint profile of a short pad extending 0.004 inches beyond the HCC package is shown in Figure 42a. This solder joint results in a very short, stubby fillet which is more like a column than a solder fillet.

The long pads result in a horizontal solder joint with most of the solder drawn out on the pad as shown in Figure 42b.

Figure 42c represents the optimum pad shape resulting in an ideal solder fillet with the fillet radius extending vertically and horizontally about equally (also shown in Figure 43). This pad is similar to the 32 terminal HCC pads.

Reevaluating the temperature cycle test results in Figure 37, it is clear that, had the two center pads of the 24 terminal HCC been closer to those in Figure 41 (protruded farther from the HCC), they would not have failed as early. Suotracting the short solder joint failures from the 24 pad HCC failures would bring the 24 pad HCC failures to a value less than the 32 pad HCC's, which is what would be expected.

The solder under the HCC's was measured to be .5 to 1 mil thick. Having such a small amount of solder under the HCC does not lengthen the life of the solder joint. Stresses are not absorbed and, therefore, matching the CTE's of the substrate and HCC becomes imperative for prolonged life of the solder connection.

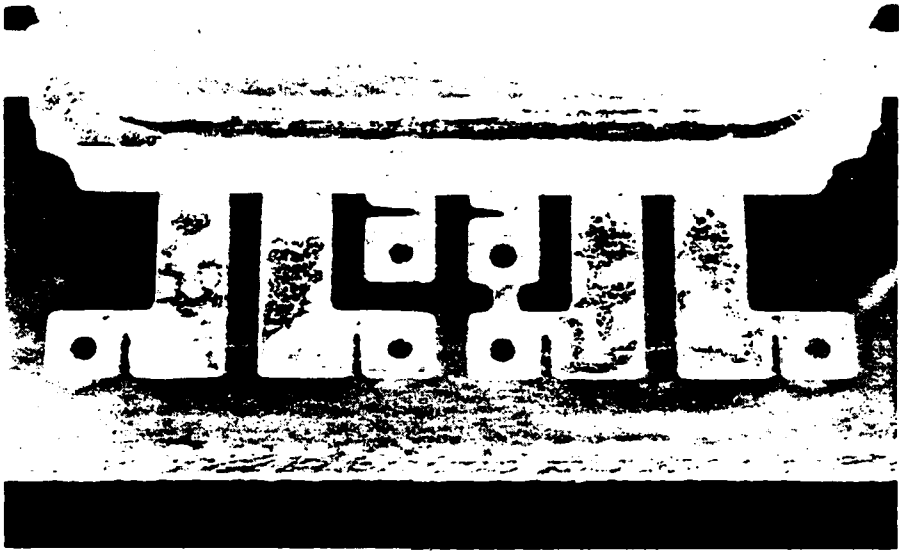


Figure 39. 24 Terminal HCC Pad Layout

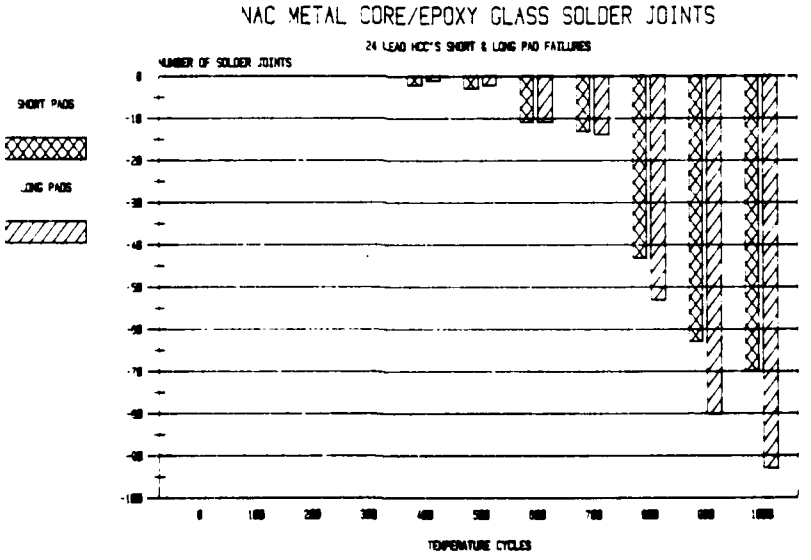


Figure 40. Metal Core Epoxy Glass 24 Terminal
Short and Long Pad Failures

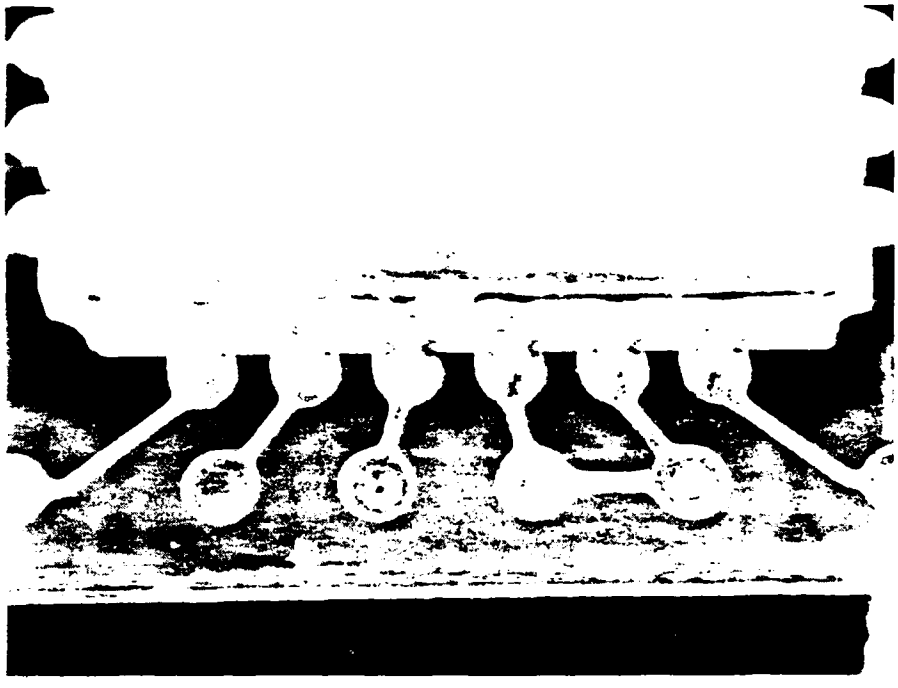
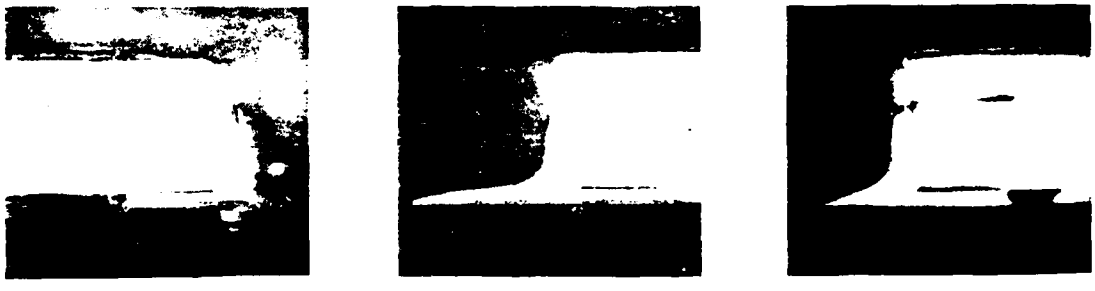


Figure 41. 24 Terminal Preferred Pad Layout



a. b. c.

Figure 42. Solder Pad Configurations

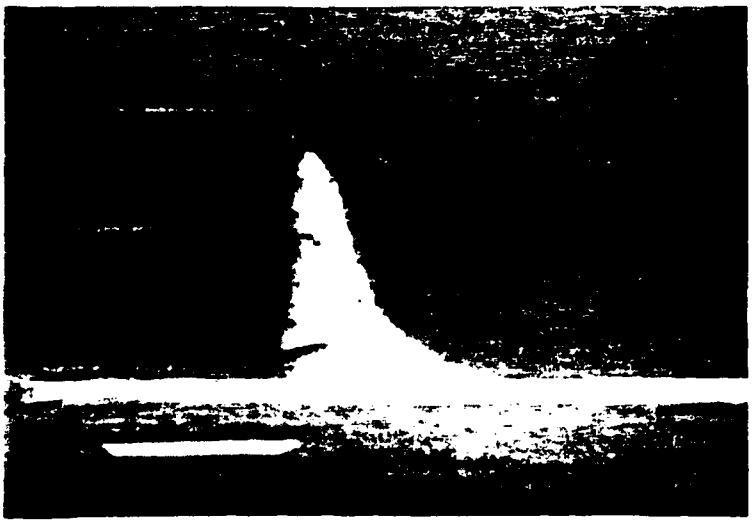


Figure 43. Good Solder Joints

8.2.4 PLATED-THROUGH HOLES AND CONNECTOR JOINTS — METAL CORE

The only PTH failure was encountered at 400 cycles and was thought to be a PTH located in the continuity circuit of one of the 14 terminal HCC's. After microsectioning the suspected PTH, it was found that the failure was the PTH which connects the connector pad to the 14 terminal HCC. In Figure 44 the non-continuous PTH wall is shown. This failure was caused from Z axis expansion. Adding non-functional pads to the PTH's would eliminate the large slug of epoxy and help control the Z axis expansion while eliminating the PTH barreling. A good PTH is shown in Figure 45.

The connector failures started at 300 cycles. The two failures were located near the end of the row of connector joints. Though the substrate directly below the connector joints was not stabilized, allowing it to expand and contract along with the connector, the end connector joints still failed. A greater distance between the Alloy 42 stabilizing planes and the connector interface is expected to resolve the connector failures. Figures 46 and 36 show a failed connector joint and a good connector joint, respectively.

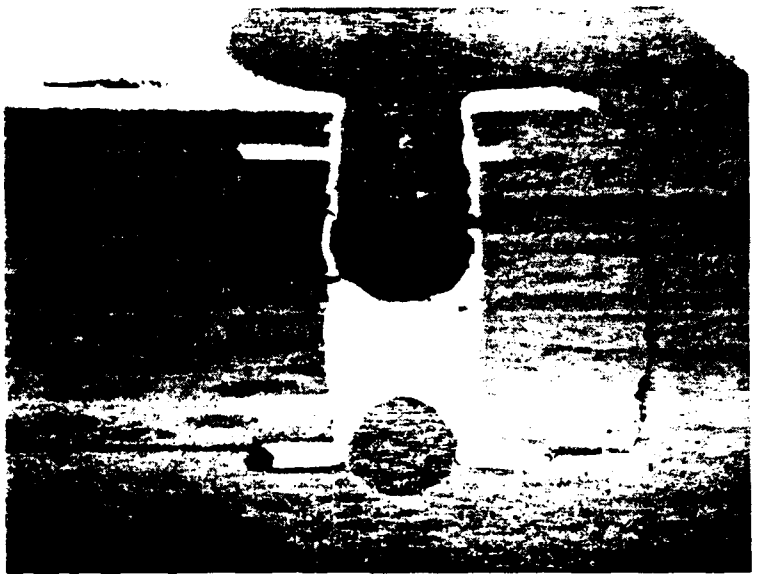


Figure 44. Failed Plated-Through Hole

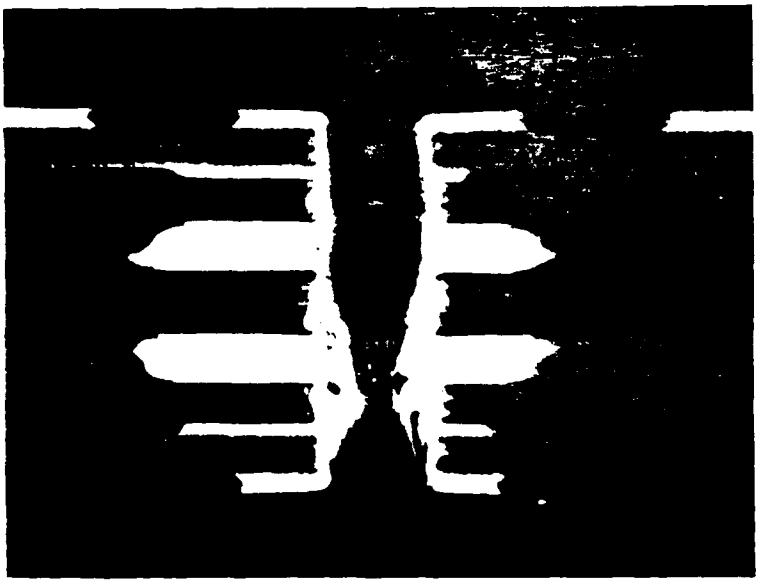


Figure 45. Good Plated-Through Hole

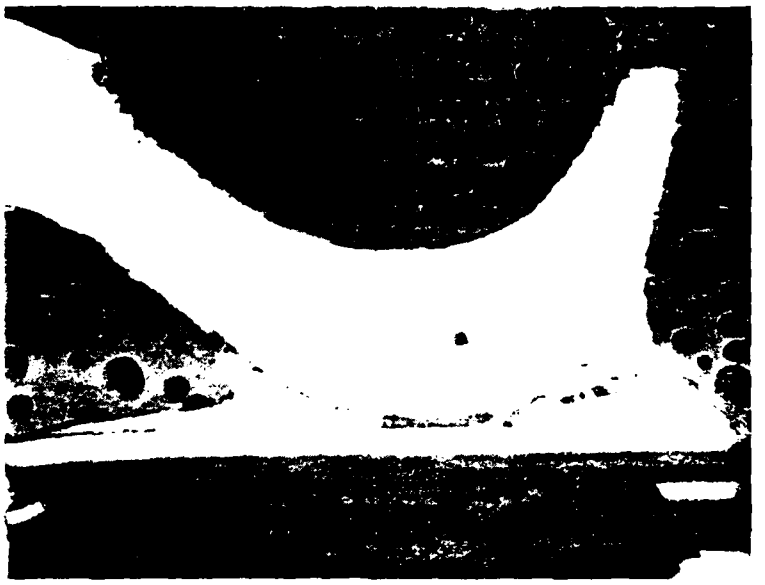


Figure 46. Failed Connector Solder Joint

APPENDIX A

1.0 SCOPE

This test program will provide NAC the opportunity to evaluate the applicability of the newly developed GE metal-core epoxy-glass multilayer board structure to the Standard Electronic Module Format B configuration. The test report shall include but is not limited to; test method description, temperature cycle test data, solder joint failure analysis and general conclusions which will demonstrate the feasibility of the GE material functioning reliability. The test plan flow chart may be seen in Figure A—1.

2.0 PWB FABRICATION

2.1 Three (3) flats of metal-core epoxy-glass PWB materials will be laminated per Figure A—2 using typical multilayer board (MLB) epoxy-glass laminating processes. Each MLB flat shall have five (5) SEM Format B MLB's designed to interface with the 0102—710 frame. MLB flat configuration is illustrated in Figure A—3.

2.2 One (1) flat of epoxy-glass PWB materials will be laminated per Figure A—4 using typical MLB epoxy-glass laminating processes. Component layout and interconnection will be identical to the metal-core epoxy-glass configuration.

3.0 PWB PROFILING

3.1 PWB profiling will utilize the routing process. PWB's will be separated from the flat and profiled simultaneously. Each PWB will be identified with flat number and PWB location in the flat.

4.0 QUALITY ASSURANCE

4.1 PWB's (one from each flat of PWB's) will be visually and dimensionally inspected per MIL—P—55110C, Paragraph 4.7. The following features shall be inspected:

a. Plated-through hole and etchback visual examination.

b. Annular ring (external layer), dielectric layer thickness, undercutting and conductor overhang dimensional tests.

c. Inspection of the termination point of Alloy 42 for delamination.

4.2 PWB samples will be cut in half across their smaller dimension thereby providing test samples for the two thermal shock tests.

4.3 Thermal shock tests — Samples will be thermally shocked and stressed to verify the plated-through hole integrity and quality of adhesion between each of the layers.

4.3.1 A hot oil or hot wax test will be performed on one of the halves of each PWB per MIL—P—55640A, Paragraph 4.7.5.

4.3.2 A solder float test will be performed on the remaining halves of the PWB's per MIL—P—55110C, Paragraph 4.8.7.

4.4 Visual and dimensional inspection (see Paragraph 4.1).

4.4.1 If PWB inspection reveals a failure, the flat to which that PWB originated from is considered unacceptable. A new flat will be fabricated and Quality Assurance tests shall be repeated.

4.4.2 If no failures are evident, module fabrication will begin.

5.0 MODULE FABRICATION

5.1 Chip carrier terminals will be tinned using the following process.

5.1.1 Clean the chip carrier terminals with permathane, acetone, and alcohol rinse. Each device is then fluxed with Alpha 100 flux or equivalent.

5.1.2 Terminals are tinned by dipping them in a solder pot for approximately 4 seconds using 63/37 solder at 230°C.

5.1.3 Clean chip carriers with permathane, acetone, and alcohol rinse to remove flux residue.

5.2 PWB lead tin reflow process shall be per the process described in Paragraphs 5.2.1 thru 5.2.3.

5.2.1 Clean the PWB surface with an ultrasonic trichlore/aicohol process. Alpha 100 flux or equivalent shall then be applied to the PWB surface.

5.2.2 Reflow the PWB's using a two (2) zone Brown Conveyer Reflow Solder Machine with 130 °C – 230 °C temperature zones. A vapor phase or infrared reflow process may be substituted pending the status of process development at the time of PWB assembly.

5.2.3 Clean PWB surface using an ultrasonic trichlore/alcohol cleaning process.

5.3 PWB's will be assembled with chip carriers in the configuration as shown in Figure A–5.

5.3.1 Chip carriers will be located on their respective pads and will be reflowed to the PWB using Brown Reflow Solder Machine with 230 °C. During the soldering process, a forming gas (90% nitrogen, 10% hydrogen) is flooded over the PWB to minimize solder oxidation. Vapor phase solder may be utilized for this process pending vapor phase process development progress at the time of component assembly.

5.3.2 Flux is not used for this process, therefore, cleaning is not required after this operation.

5.4 Bonding of the PWB to the Standard Electronic Module 0102–710 frame will take place as described in Paragraph 5.4.1.

5.4.1 The underside of the PWB (non-component side) will be coated with GE RTV silicone adhesive using the following process:

Apply two (2) portions of RTV silicone (approximately 1/2 inch dia. x 3/16 high) toward one end of the PWB. A flexible rubber squeegee, held at 30 ° angle with the horizontal, will be used to spread the RTV silicone to a thickness of 4 to 6 mils. Two (2) passes will be made – one from each end of the PWB toward the center. Caution will be taken to ensure complete adhesive coverage of the entire PWB surface. Immediately following the adhesive application, the PWB will be placed in the 0120–710 frame and slight pressure will be applied to ensure good bonding.

5.4.2 Following completion of the bonding process, the connector terminals will be soldered to the PWB using 63/37 solder.

5.5 A visual inspection will be performed after completion of the module assembly with a 7–10 power microscope. Photographs will be taken of the

various inspected areas before, during, and after testing. Inspection shall include:

a. Bond joint inspection — Check for adhesive fillet along the edges of the PWB.

b. Solder joint inspection — Check for good fillets, good solder wetting, no cracks, and no cold solder joints. Touch up will be performed as necessary using 63/37 solder paste as the means of adding additional solder to a solder joint.

6.0 THERMAL CYCLE EVALUATION TEST

6.1 The PWB specimens will be thermally cycled using a Ransco 7107—1 thermal shock chamber with 6 kilowatt heating and 15 horsepower cascade refrigeration. Figure A—6 depicts the Ransco 7107—1 thermal shock chamber.

6.2 PWB specimens shall be temperature cycled between —55 ^{o}C and +125 ^{o}C for 1000 cycles. The temperature chamber will dwell at each temperature extreme for twenty (20) minutes, resulting in the PWB assembly stabilizing at that extreme approximately 7—10 minutes. Chamber temperature and module temperature as a function of time are depicted in Figure A—7 and A—8 respectively.

6.3 Test samples will be electrically monitored to detect an open circuit using a 14 station GEOS continuity tester. This monitor equipment will indicate which PWB and at what cycle time a particular PWB failed. Figure A—9 depicts the 14 station GEOS continuity tester.

6.4 Visual solder joint inspection will take place at 50, 100, 200, 300 and 400 cycles. Inspection will take place thereafter at 1000 cycles or failure, whichever occurs first. A total of six (6) inspections shall be performed. Inspection shall be done under a microscope (7—10X magnification) and microsection photographs will be taken of good and suspect solder joints when feasible.

6.5 Failures will be located by utilizing the design characteristics of the PWB circuitry. Each chip carrier has terminals interconnected as defined in Figure A—10. Each chip carrier is connected to the connector by means of 5 circuit paths (1 in, 1 out, and 3 test points). Electrical shorting of selected test points facilitates identifying the failure area. Failure shall be defined as an electrically open solder joint connection. Experience indicates most failures are intermittant. Therefore, failure identifications will be performed in the test chamber.

6.6 Sample failing to successfully complete thermal cycle tests will be visually inspected.

6.6.1 Chip carrier solder joint inspection — A 30 power microscope will be used to inspect solder joints for stress cracks or joint separation. Artist sketches and/or photographs will be utilized to record these results.

6.6.2 Connector interface inspection — The connector to PWB interface will be inspected for discontinuity or stress cracks using a 30 power microscope. Artist sketches and/or phtotographs of the inspection results will then be performed.

6.7 A microsection of the particular failure to further identify the mode of failure will be accomplished. A microsection of the plated-through holes will be performed as described in MIL—P—55110C, Paragraph 3.8.1.

6.8 Samples successfully completing thermal cycle tests will be visually inspected for solder joint quality using a 30 power microscope.

6.9 Microsections of good and suspect solder joints and plated-through holes will be performed to depict quality of the interconnections after stress testing. Inspection of PWB at discontinuity paths of Alloy 42 shall also be accomplished.

7.0 REPORTS

Interim and final report will include documenting test methods, test results, failure analysis, conclusions, and recommendations.

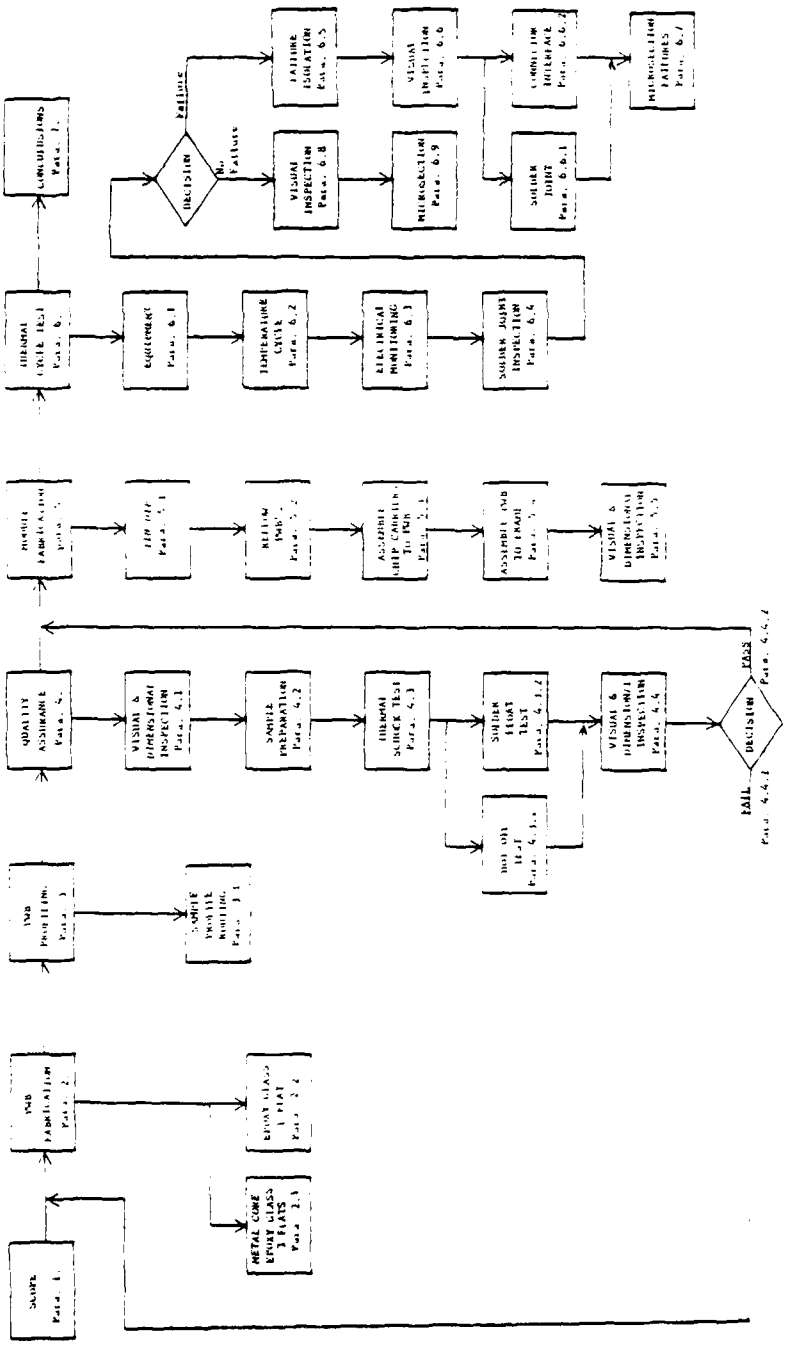


Figure A—1. Test Plan Flow Chart

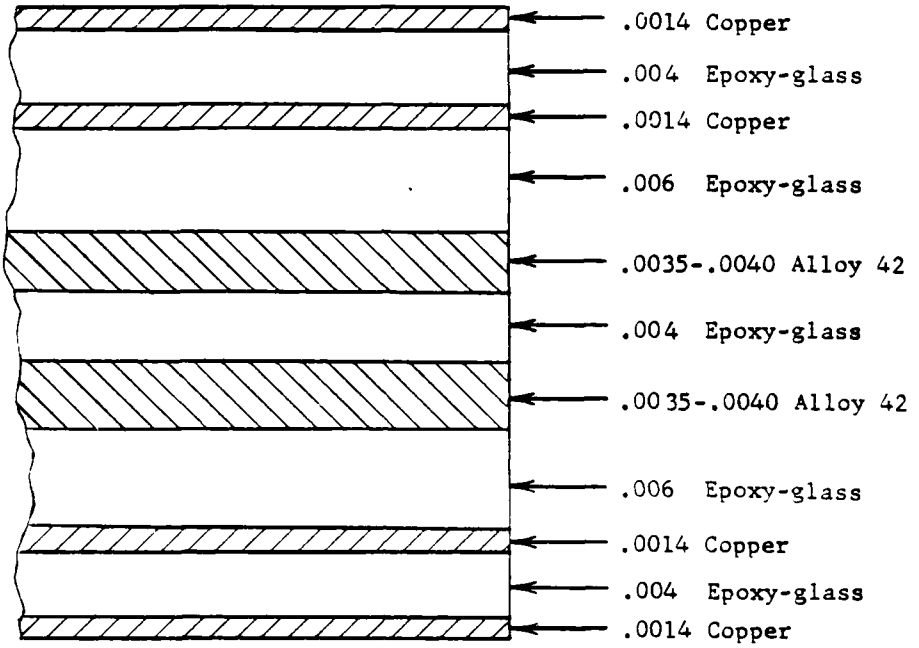


Figure A—2. Metal Core/Epoxy Glass MLB Lamination

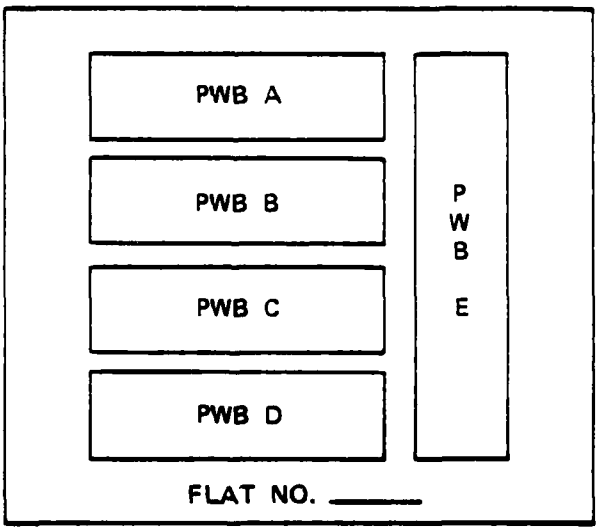


Figure A—3. MLB Flat Layout

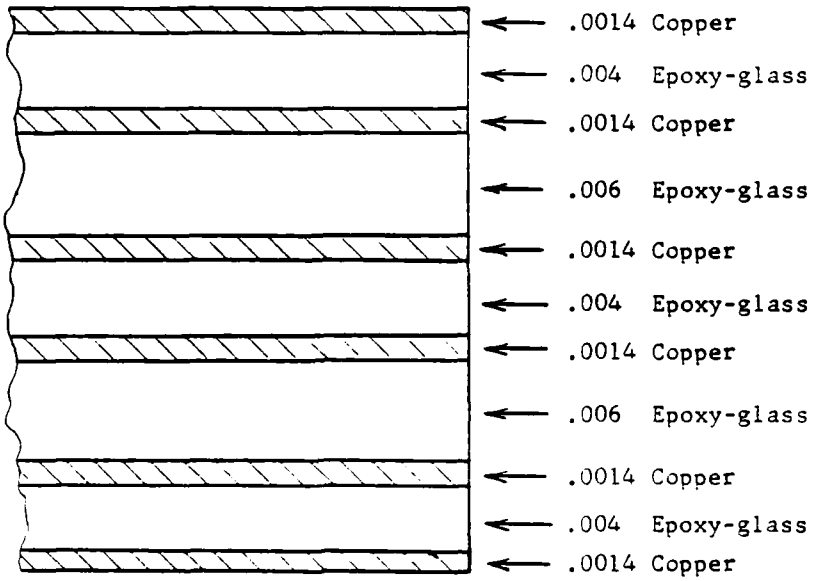


Figure A—4. Epoxy Glass Lamination

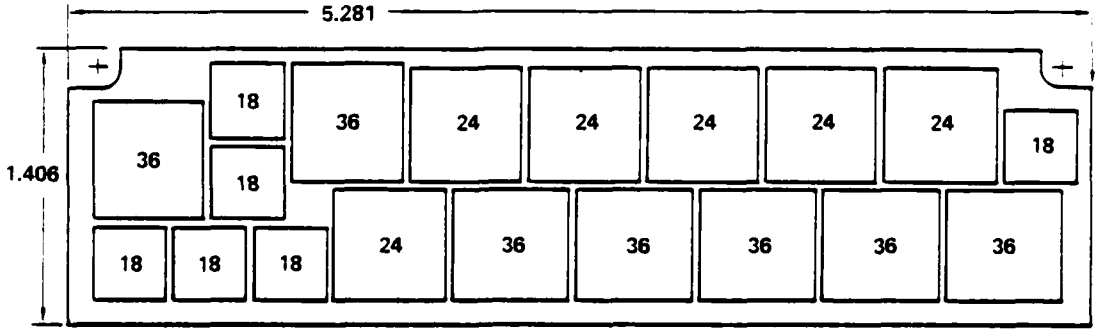


Figure A—5. PWB Chip Carrier Configuration

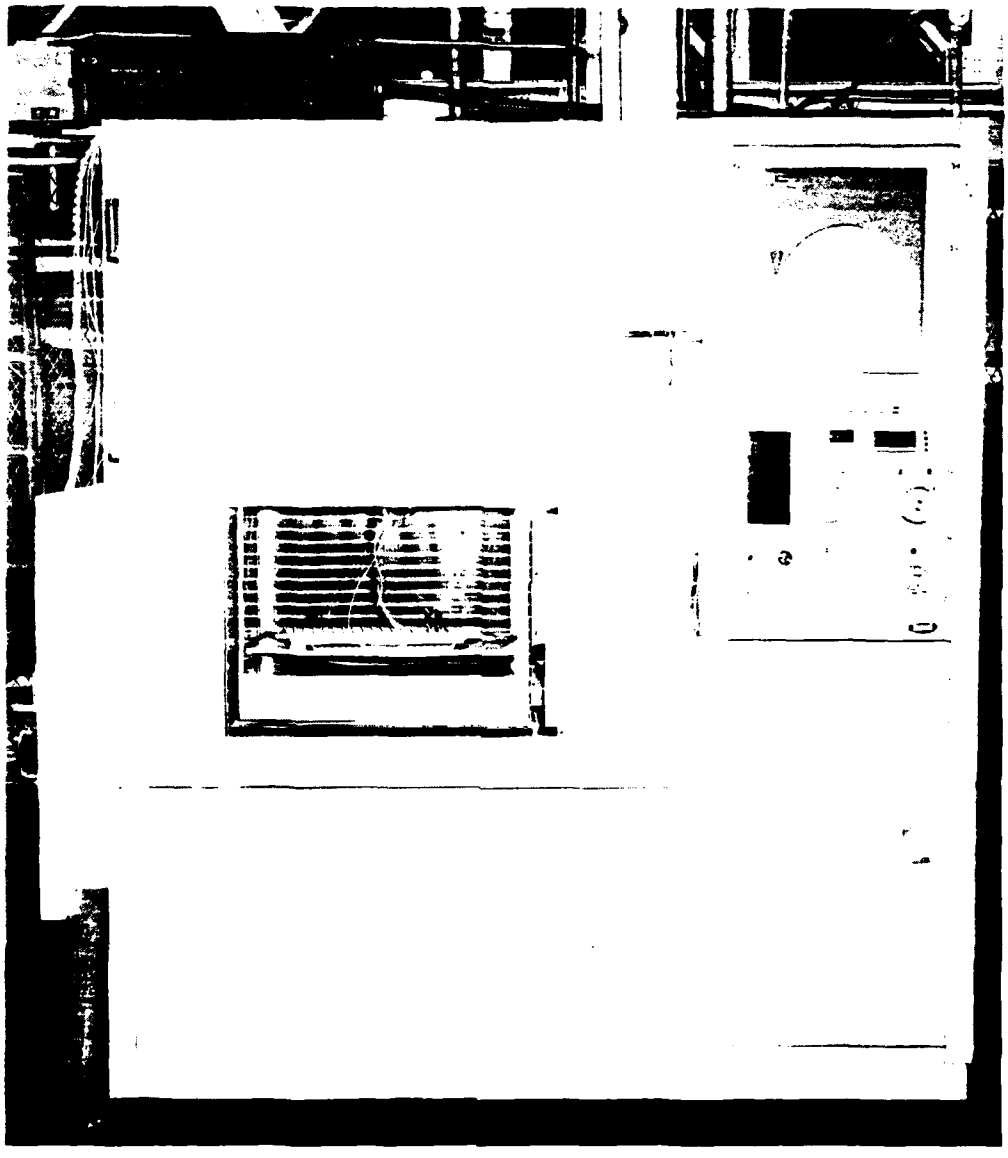


Figure A—6. Ransco Thermal Cycle Chamber

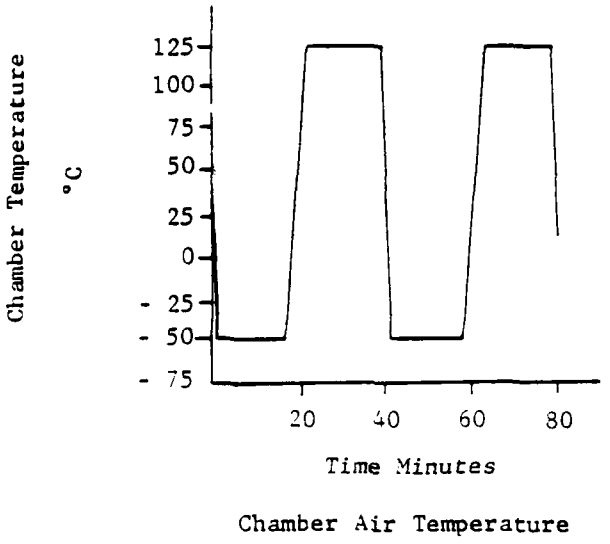


Figure A—7. Chamber Air Temperature

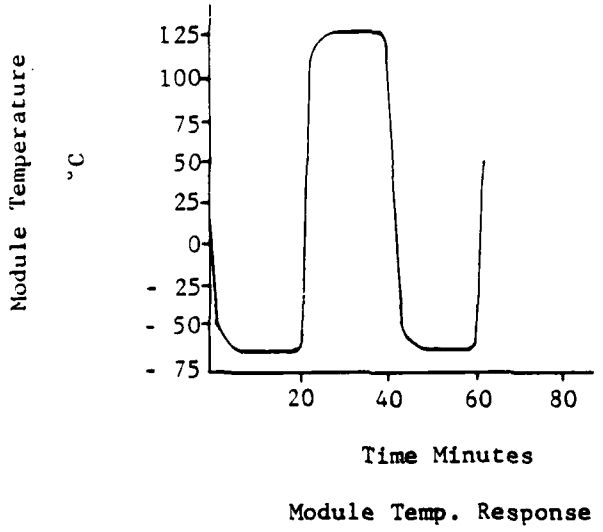


Figure A—8. Module Temperature Response

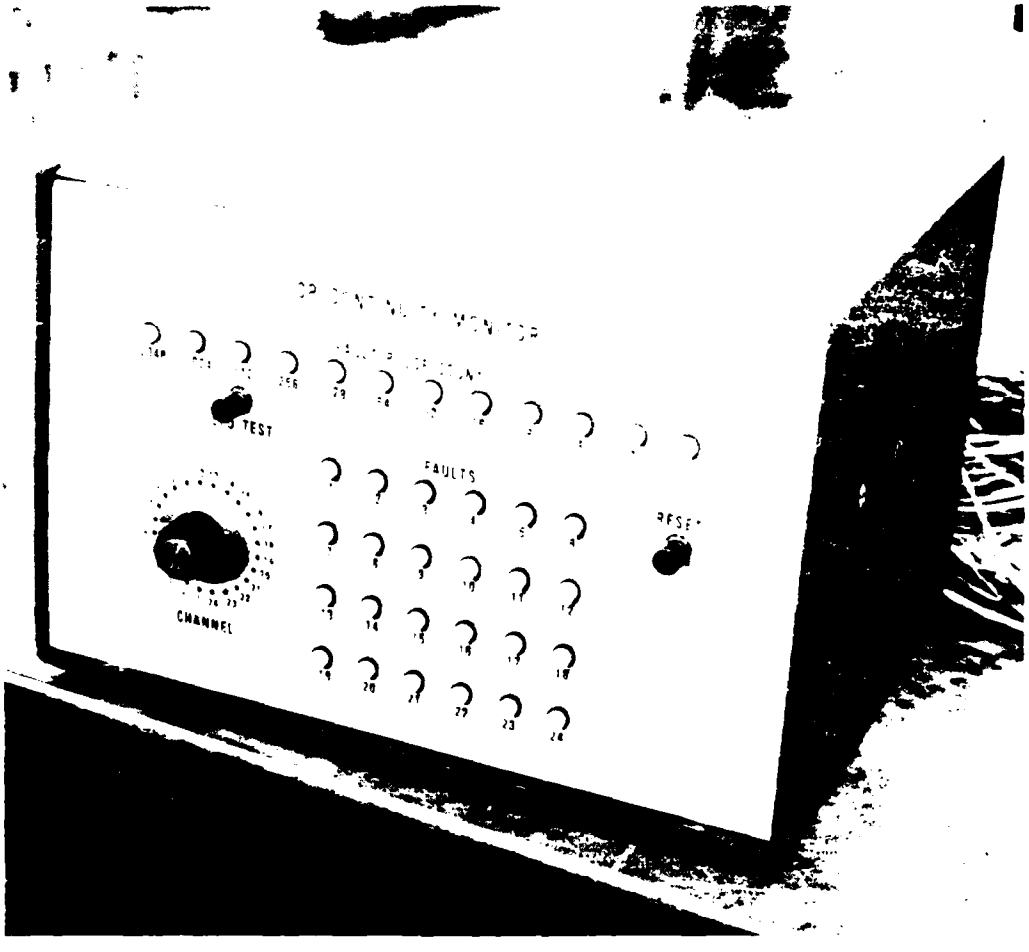


Figure A—9. GEOS Continuity Monitor

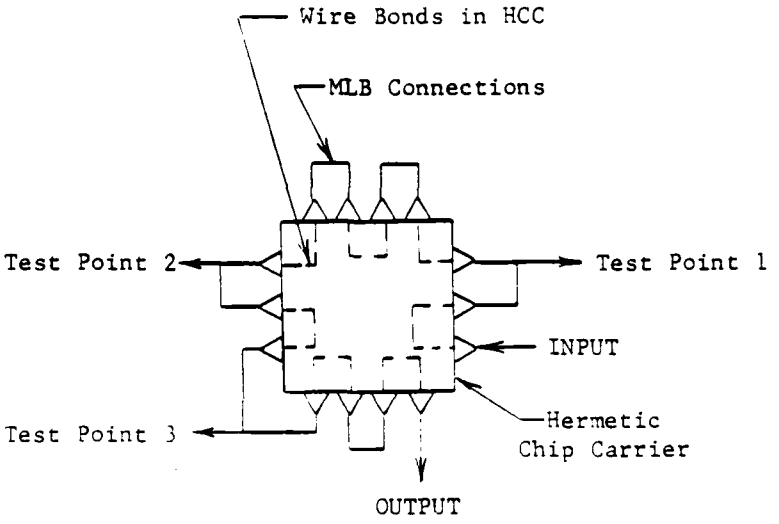
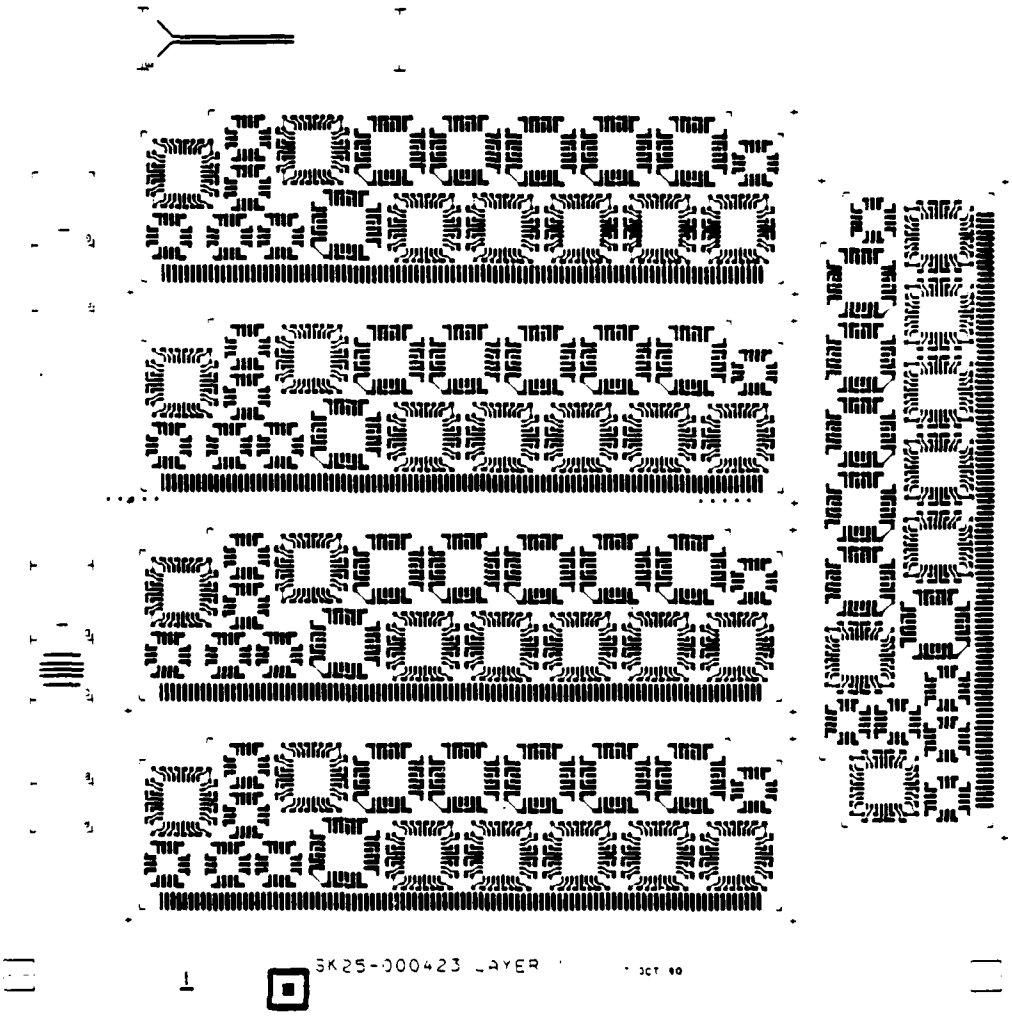
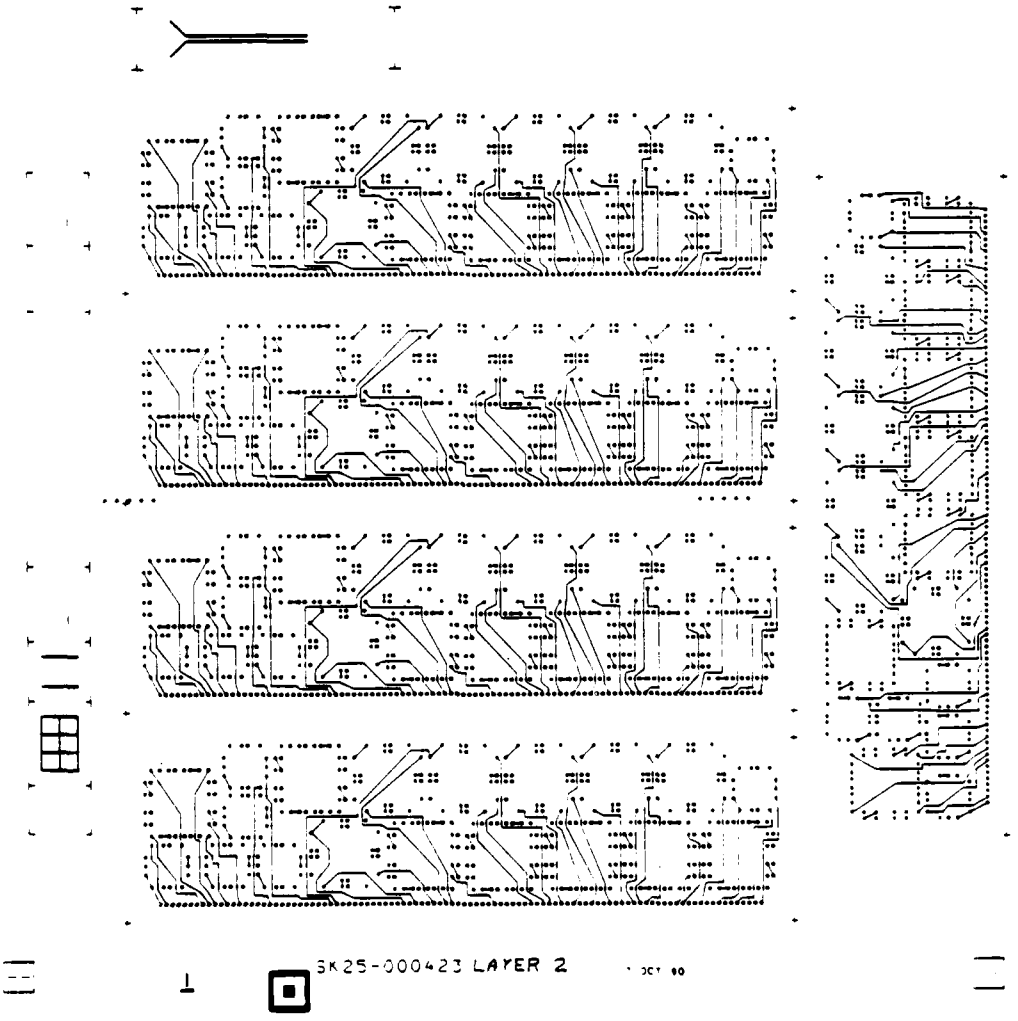


Figure A—10. Typical Chip Carrier Interconnection

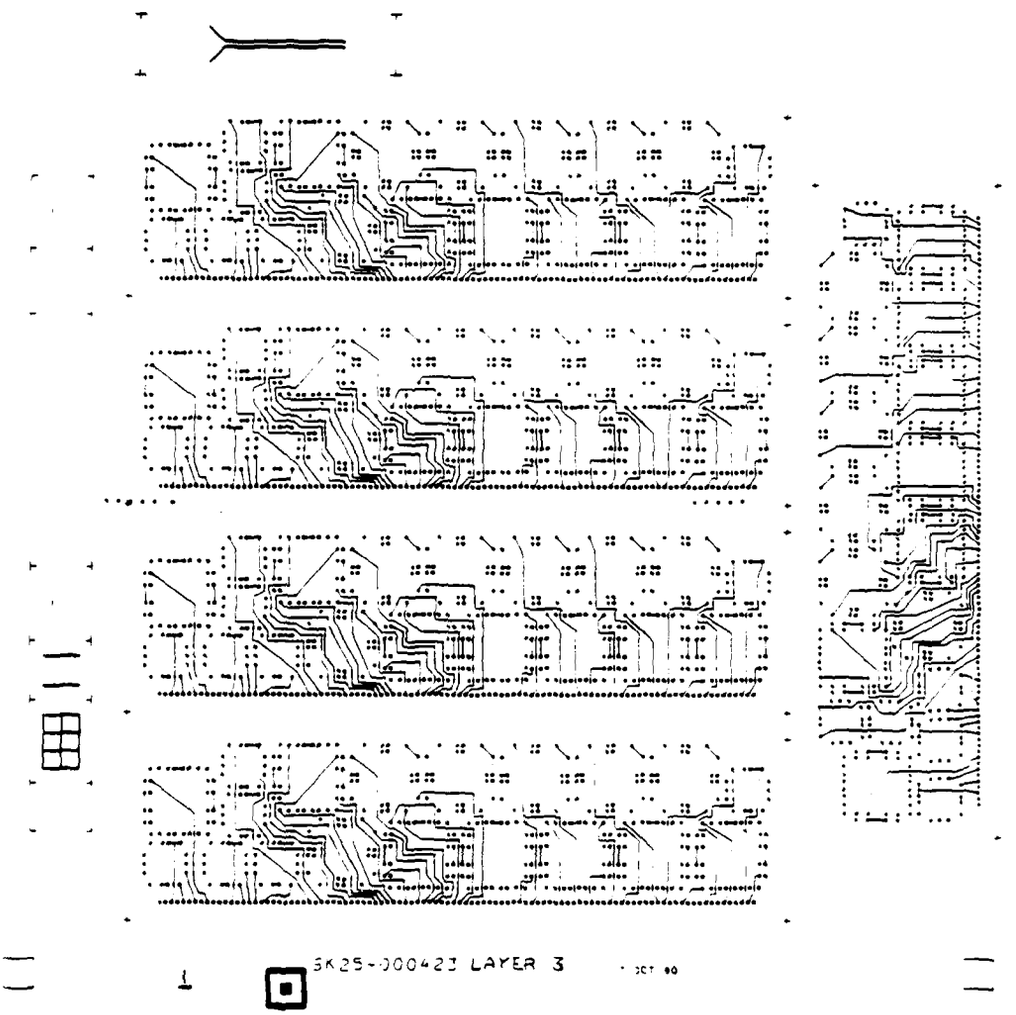
Test Module Artwork



Test Module Artwork



Test Module Artwork



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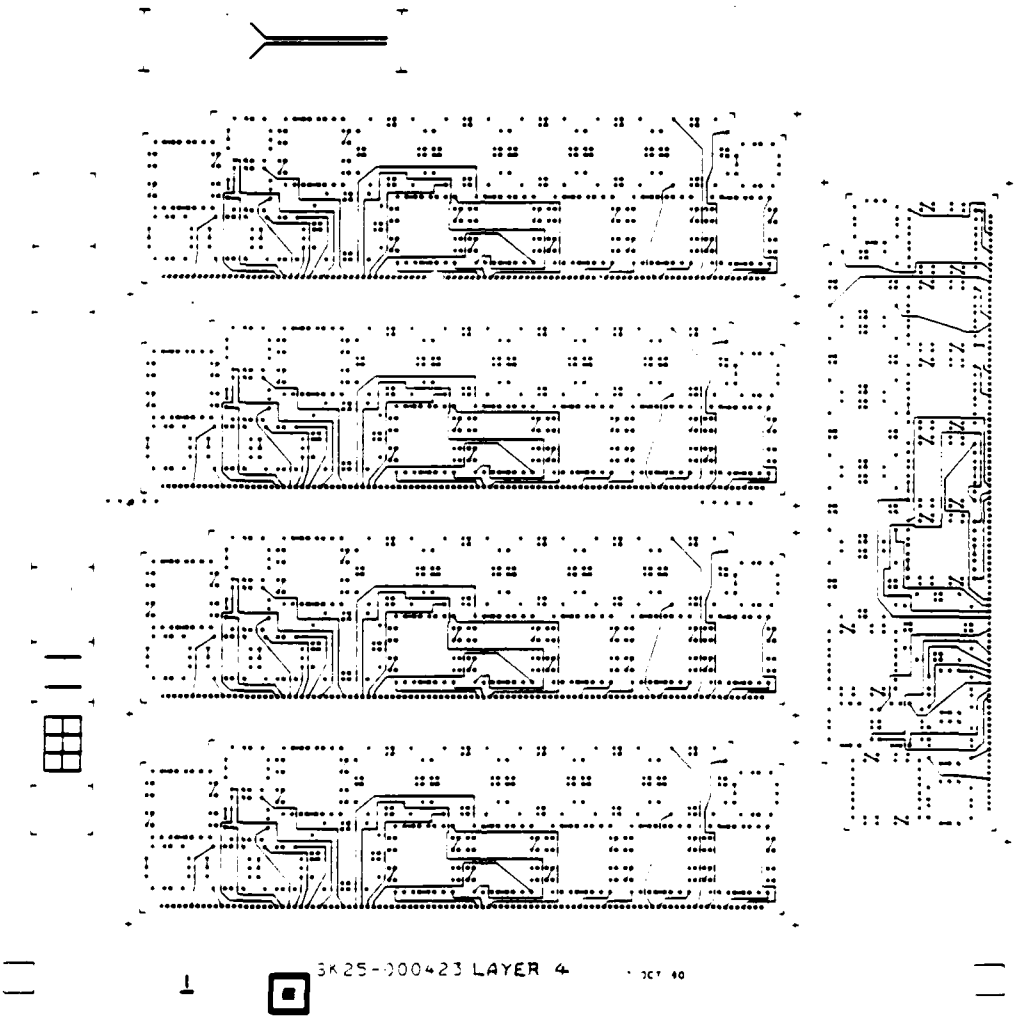

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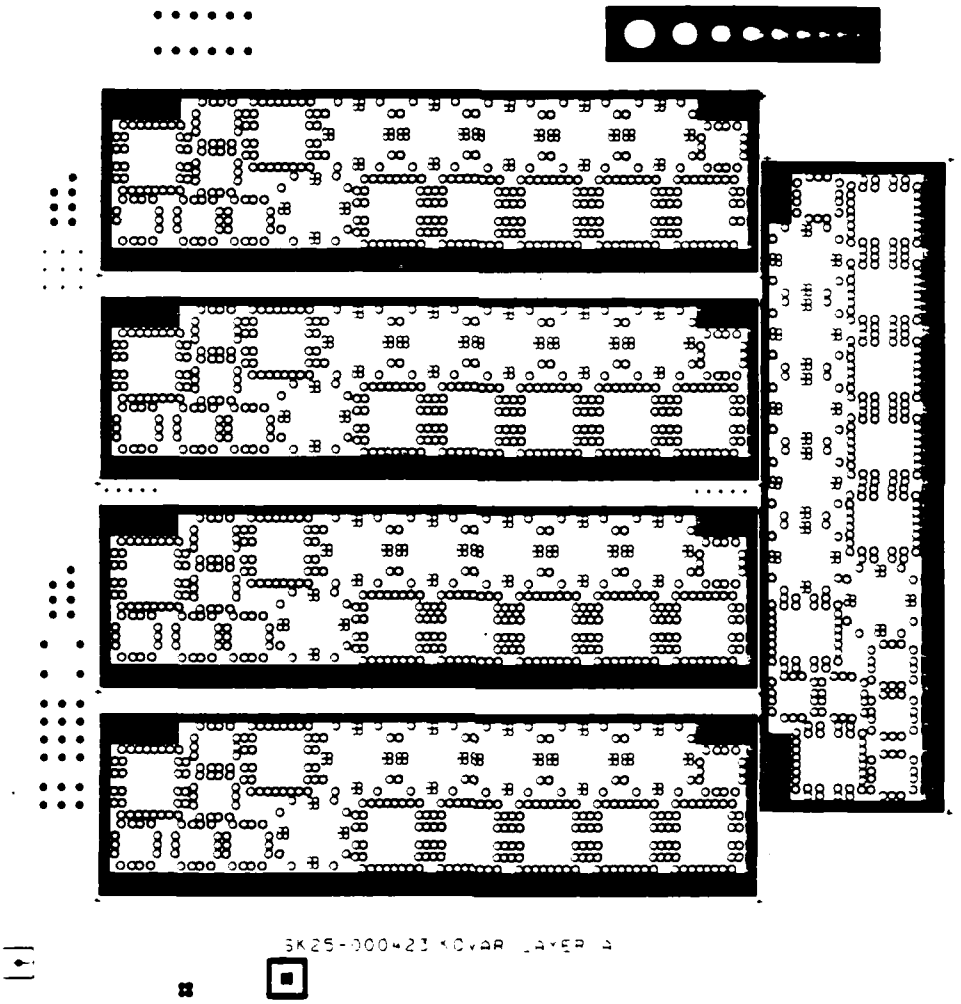

APPENDIX B

BACKGROUND

In terminating chip carriers, conventional pad designs, such as those used for flat-packs, were not satisfactory because of the PTH siphoning solder off the pads (see Fig. B—1a). To remedy the solder-hole problem a necked-down area was added to each pad. This neck down acted as a solder dam to retain solder on the chip carrier pad areas for the chip carrier fillets (see Fig. B—1b). Test boards were manufactured, assembled, and temperature cycled. Though the solder was not siphoned into the PTH, uneven fillets were still present, causing premature failure especially in those with a low amount of solder. To provide a more uniform fillet formation, the pad geometry was redesigned to yield uniform solder pad areas.

PAD OPTIMIZATION

A study of the chip carrier pad and hole locations were undertaken to optimize the chip carrier solder joints. The study began by evaluating the hole locations. Main areas of concern included: (1) how many runs fit under each chip carrier — between the PTH's on internal layers, (2) the overall size of the chip carrier footprint. After considering different combinations of hole spacing and overall footprint layout, optimum number of runs under the chip carrier-to-footprint real estate ratio was established.

Chip carrier solder pads were designed to carry out two separate functions. First, the pad must enhance the solder joint by providing optimum height to length fillet ratio. Second, the pad design should facilitate layout and photoplotting. A basic design was implemented taking into account each of these two criteria.

To determine the optimum length pad, different pad lengths were evaluated by fabricating and testing samples. The length of the pads under the chip carrier were kept constant; only the portion extending from the chip carrier was varied. Artwork was generated and PWB's were fabricated having these six different pad lengths .044, .050, .055, .065, .075 and .085. Assembly of the chip carriers to the PWB's was accomplished in a hot oil reflow medium. Inspection and evaluation of the pad sizes after assembly showed that the .065 inch-long pads were optimum. The chip carrier pads were connected to the feed-thru holes using an .010 inch run. This run performs like a solder dam, restraining the solder flow into the hole.

This new pad-hole interconnection design was then applied to the existing PWB layout, yielding a high-density PWB with uniform chip carrier/PWB solder fillets (see Fig. B—1c.).

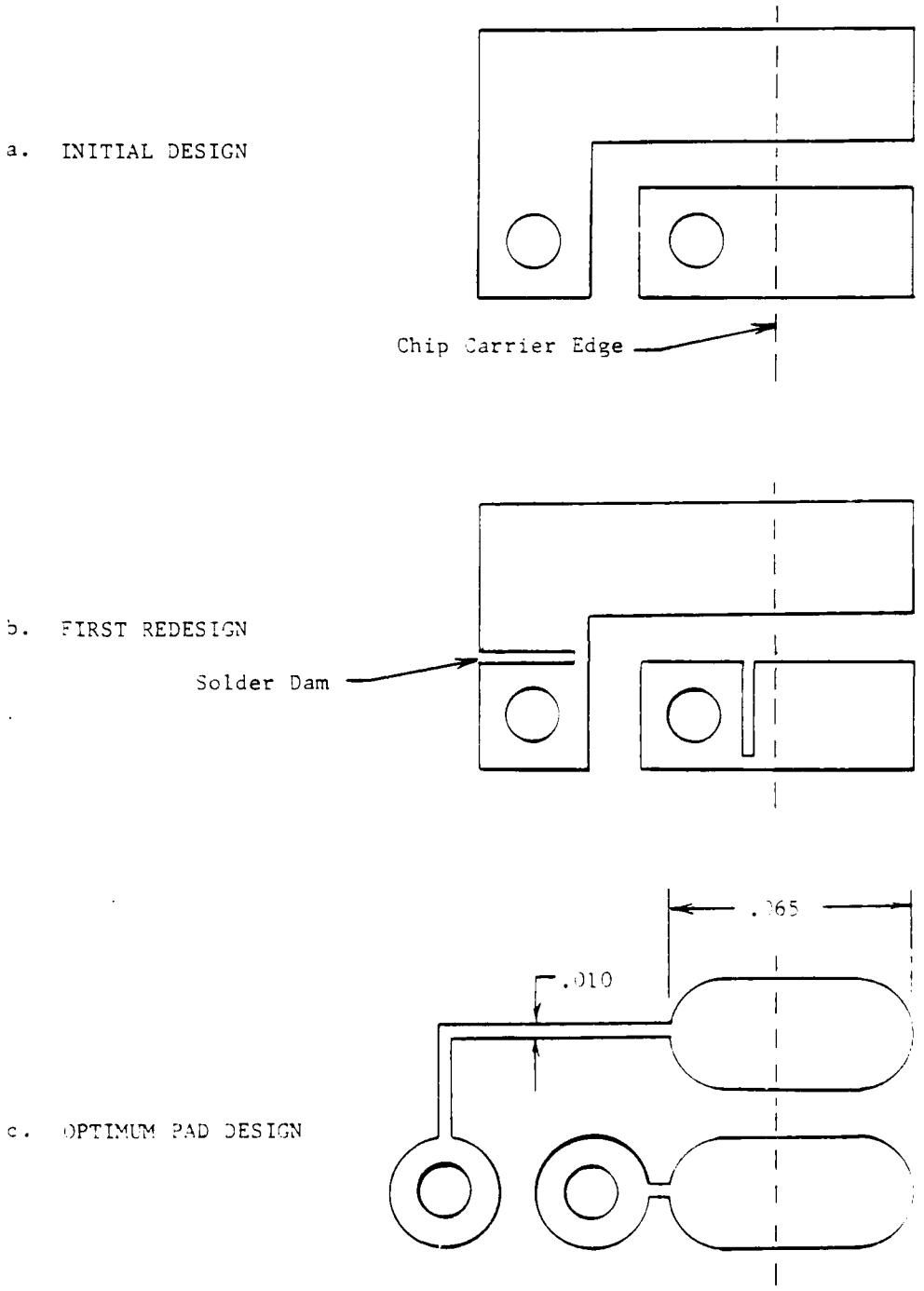

Figure B—1. Typical Chip Carrier Pads


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